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Driver v. 5.12

Interfacing FlashRunner 2.0 with INFINEON TRAVEO2

Moreno Ortolan

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INFINEON TRAVEO2 Introduction

32-bit TRAVEO™ T2G Arm® Cortex® Microcontroller

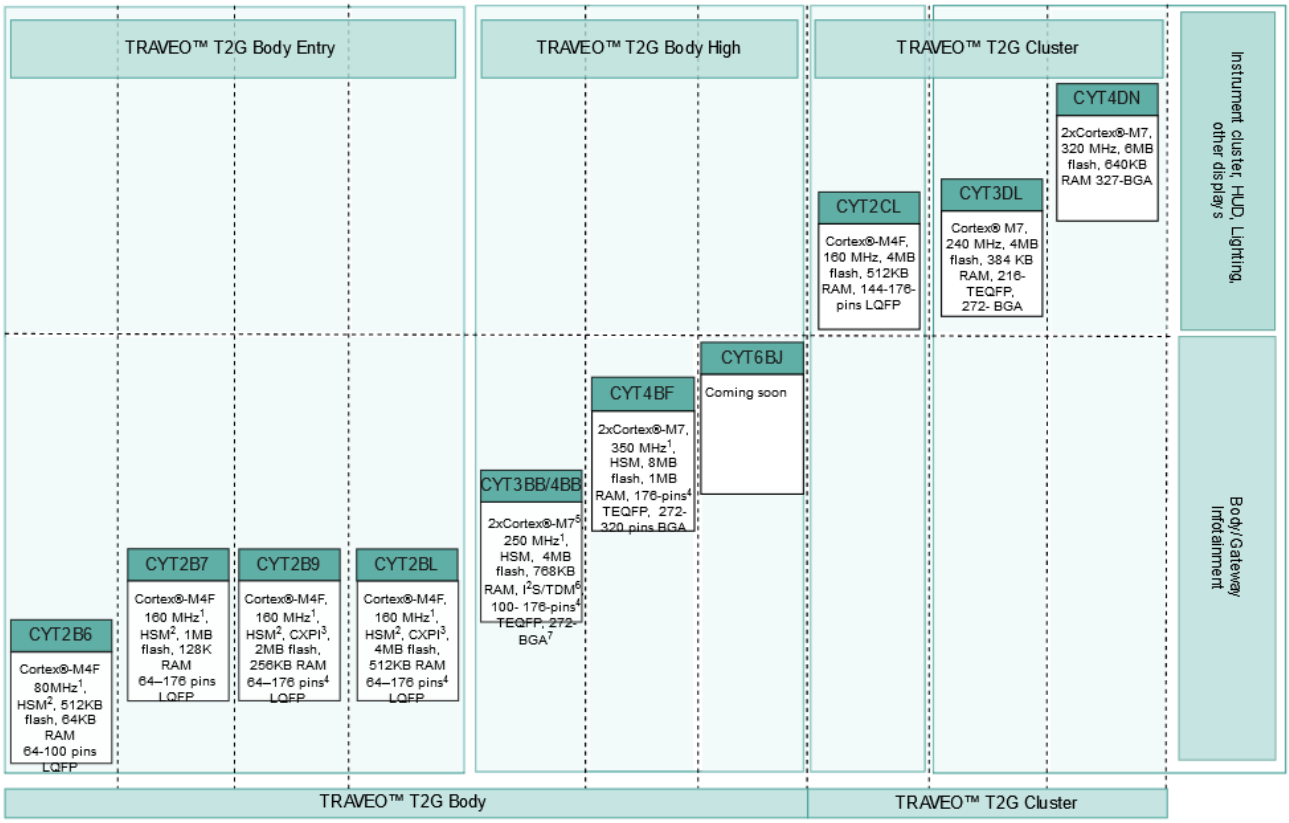
The Infineon TRAVEO™ T2G microcontrollers are based on the Arm® Cortex®-M4(Single core)/M7(Single core/Dual core) core and deliver high performance, enhanced human-machine interfaces, high-security and advanced networking protocols tailored for a broad range of automotive applications such as electrification, body control modules, gateway, and infotainment applications.

Based on the powerful Arm® Cortex® M series core in single and dual core operation it offers state-of-the-art real time performance, safety and security features. Infineon TRAVEO™ T2G MCUs are used in motor control for hybrid and electric vehicles (HEV/EV), body electronics.

Infineon TRAVEO™ T2G family builds upon the successful TRAVEO™ T1G families.

The family supports the latest in-car networks, offers high performance function optimized for a minimum memory footprint and embeds dedicated features to increase data security in the car.

TRAVEO™ T2G portfolio overview



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32-bit TRAVEO™ T2G Arm® Cortex® for Body

TRAVEO™ T2G for automotive body electronics applications offers cutting-edge performance, safety, and security features.

32-bit TRAVEO™ T2G Arm® Cortex® for Body subcategories

- › TRAVEO™ T2G CYT4BF Series
- › TRAVEO™ T2G CYT3BB/CYT4BB Series
- › TRAVEO™ T2G CYT2BL Series
- › TRAVEO™ T2G CYT2B9 Series
- › TRAVEO™ T2G CYT2B7 Series
- › TRAVEO™ T2G CYT2B6 Series

The TRAVEO™ T2G connected ready MCU family is designed for the smart world. The family offers wide scalability and network connectivity built into a single Arm® Cortex®- M4 and dual Cortex®- M7.

Performance has also been enhanced from 400 DMIPS in TRAVEO™ T1G, to 1500 DMIPS in TRAVEO™ T2G.

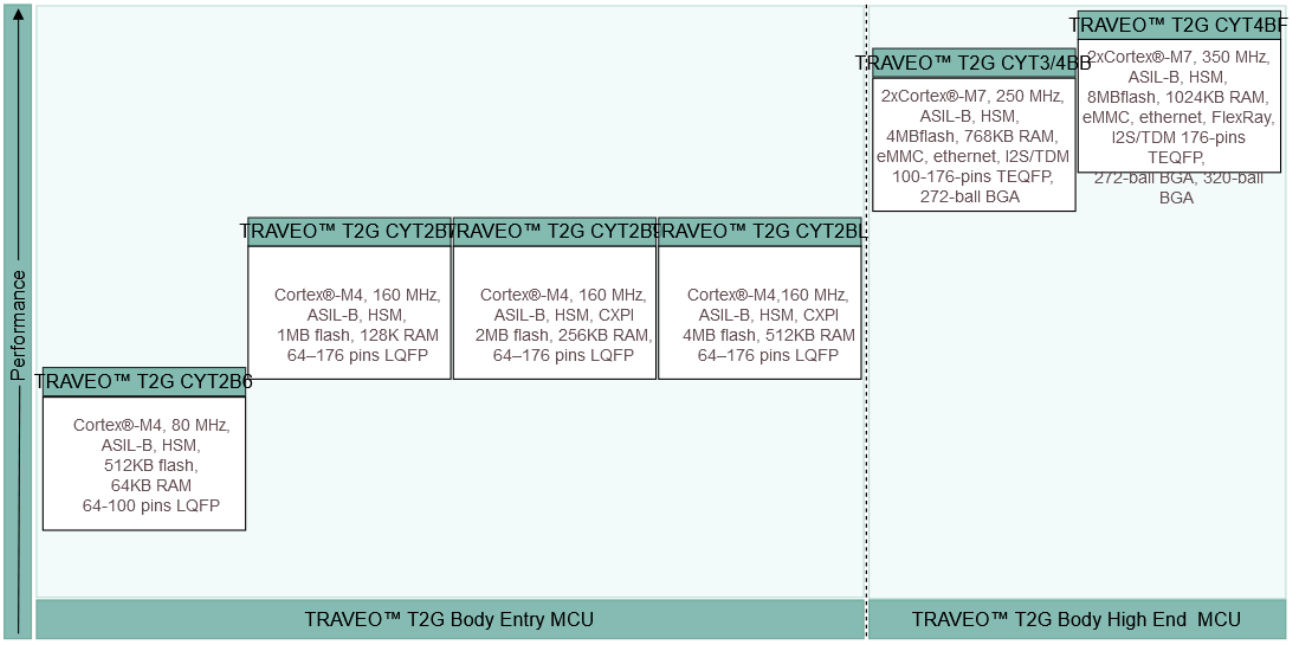
The TRAVEO™ T2G for body electronics applications also provides scalability across memory size and pin count. The IP compatibility enables customers to design and develop their systems with a single-platform MCU solution.

TRAVEO™ T2G devices have advanced security features with the introduction of HSM (Hardware security module), dedicated Cortex®-M0+ for secure processing, and embedded flash in dual bank mode for FOTA requirements.

The body family also features six power modes that enable ECUs to minimize overall power consumption.

Our MCUs come with an optimized software platform that is available for AUTOSAR MCAL (Microcontroller Abstraction Layer), self-test libraries, Flash EEPROM emulation, as well as security low-level drivers, combined with third-party firmware.

TRAVEO™ T2G Arm® Cortex® for Body portfolio



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32-bit TRAVEO™ T2G Arm® Cortex® for Cluster

TRAVEO™ T2G Instrument Cluster offers high display resolution, superior performance and multiple displays with dynamic content. All while using less power and less memory.

32-bit TRAVEO™ T2G Arm® Cortex® for Cluster subcategories

- › TRAVEO™ T2G CYT2CL
- › TRAVEO™ T2G CYT3DL
- › TRAVEO™ T2G CYT4DN

TRAVEO™ T2G automotive microcontrollers (MCU) family for Instrument Cluster with its new graphics architecture enables a more robust and feature-rich graphics engine for automotive display systems.

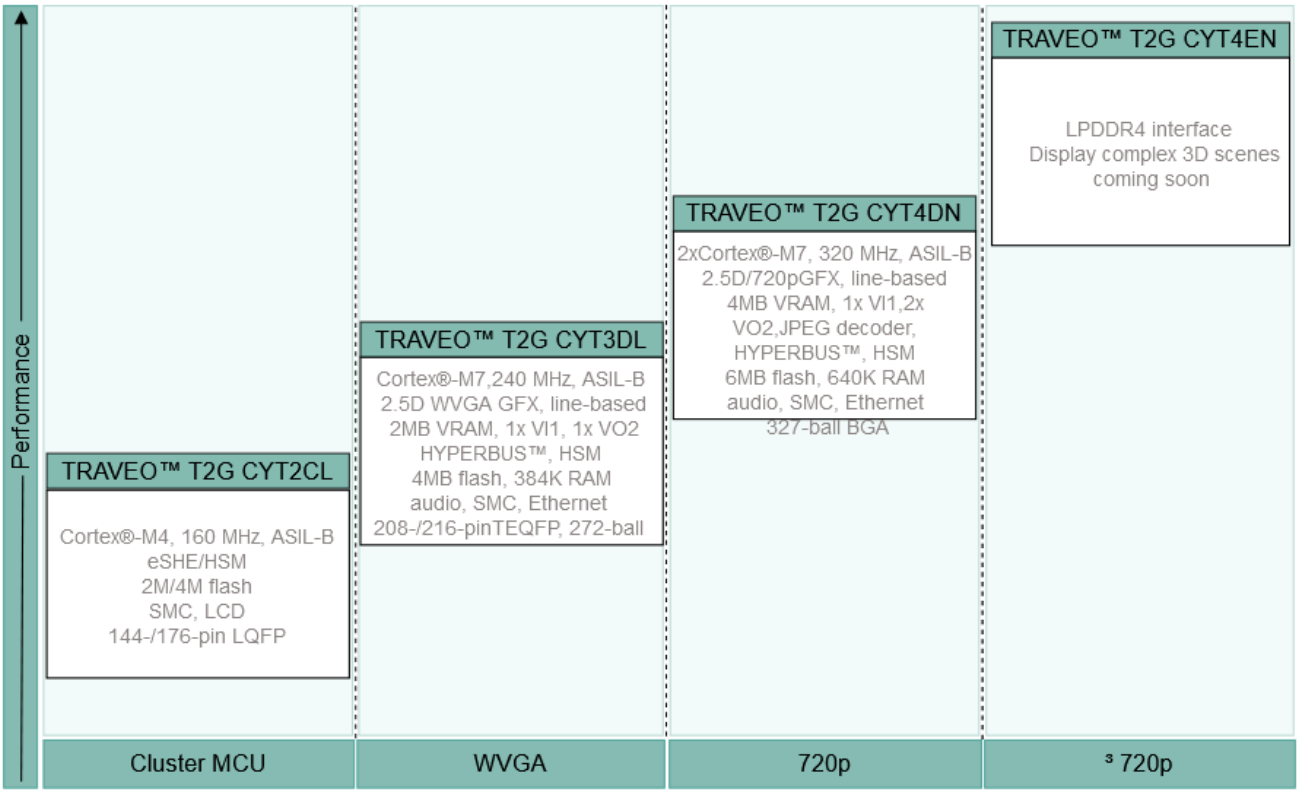
The product families provide the most extensive scalability, covering the conventional gauge instrument cluster, hybrid instrument cluster, and virtual instrument cluster.

The option of line-based operation of the graphics engine within the microcontroller minimizes the memory required for graphics processing. With the optimized 2.5D graphics engine and extended density of embedded Flash and Video RAM, TRAVEO™ T2G graphic MCU can support the virtual instrument cluster with high resolution up to 2880 x 1080.

TRAVEO™ T2G Instrument Cluster family eliminates bulky energy-hungry thermo-mechanical designs with a single platform MCU solution.
It further removes costs with innovative on-the-fly-based rendering in the integrated VRAM.

This growing family of high-performance MCUs is scalable and comes with varying configurations of ARM® Cortex® CPUs.

TRAVEO™ T2G Arm® Cortex® for Cluster portfolio



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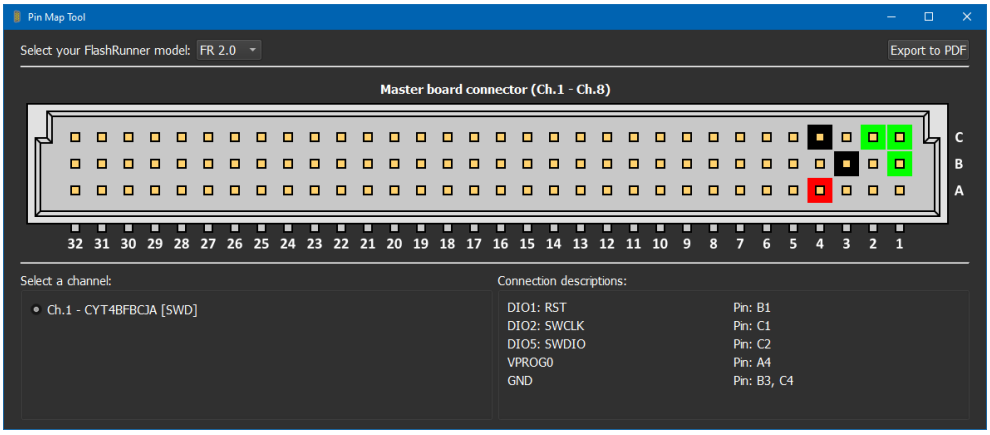
INFINEON TRAVEO2 Protocol and PIN map

TRAVEO2 devices support the SWD protocol.

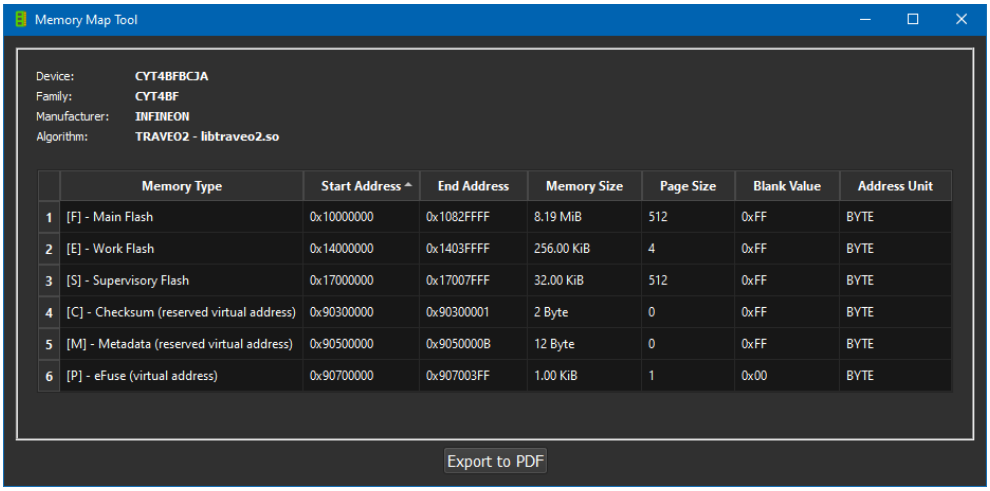
```
#TCSETPAR CMODE <SWD>
```

INFINEON TRAVEO2 PIN MAP



INFINEON TRAVEO2 Memory Map

Memory Type	Start Address	End Address	Memory Size	Page Size	Blank Value	Address Unit
[F] - Main Flash	0x10000000	0x1082FFFF	8.19 MiB	512	0xFF	BYTE
[E] - Work Flash	0x14000000	0x1403FFFF	256.00 KiB	4	0xFF	BYTE
[S] - Supervisory Flash	0x17000000	0x17007FFF	32.00 KiB	512	0xFF	BYTE
[C] - Checksum **(reserved virtual address)**	0x90300000	0x90300001	2 Byte	0	0xFF	BYTE
[M] - Metadata **(reserved virtual address)**	0x90500000	0x9050000B	12 Byte	0	0xFF	BYTE
[P] - eFUSE **(virtual address)**	0x90700000	0x907003FF	1.00 KiB	1	0x00	BYTE



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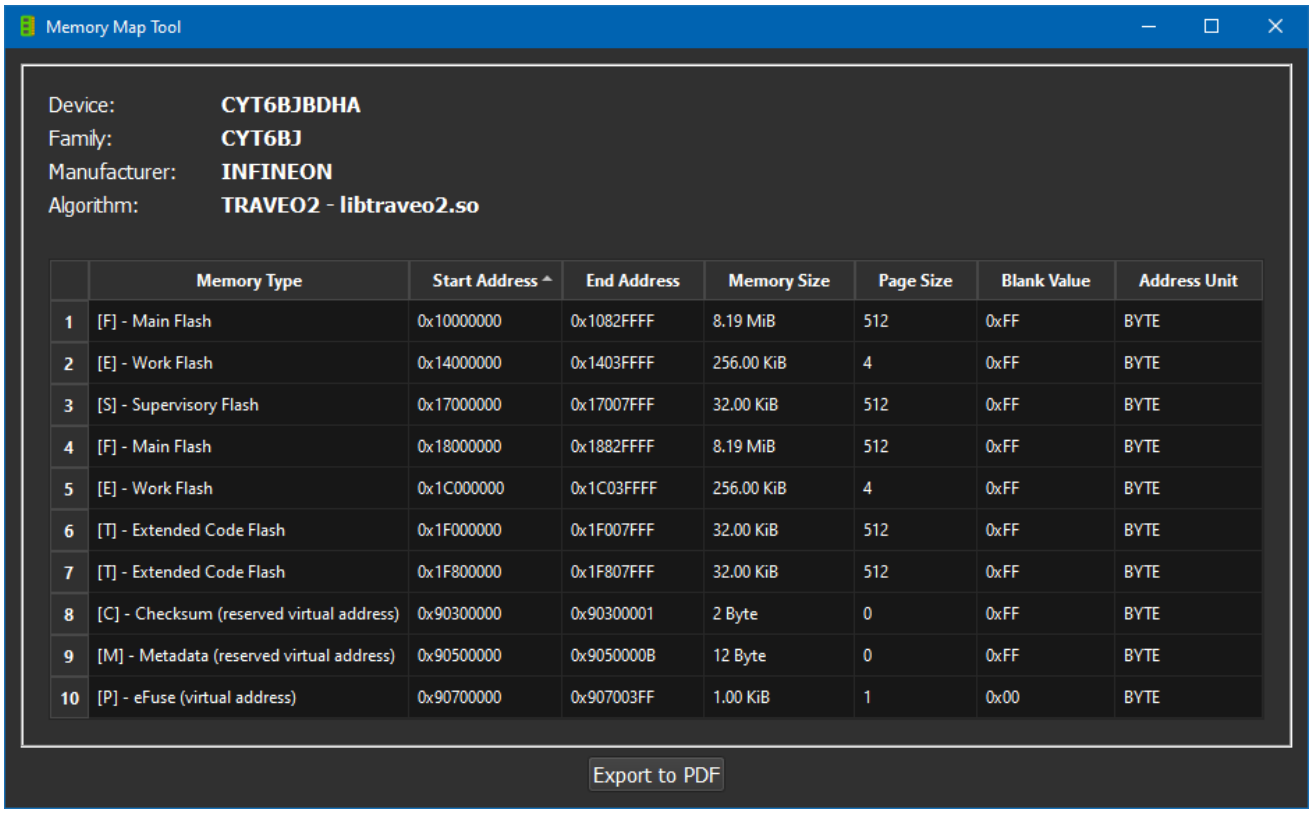
INFINEON TRAVEO2 Memory Map for Dual Controller Devices

Memory Type	Start Address	End Address	Memory Size	Page Size	Blank Value	Address Unit
[F] - Main Flash	0x10000000	0x1082FFFF	8.19 MiB	512	0xFF	BYTE
[E] - Work Flash	0x14000000	0x1403FFFF	256.00 KiB	4	0xFF	BYTE
[S] - Supervisory Flash	0x17000000	0x17007FFF	32.00 KiB	512	0xFF	BYTE
[F] - Main Flash	0x18000000	0x1882FFFF	8.19 MiB	512	0xFF	BYTE
[E] - Work Flash	0x1C000000	0x1C03FFFF	256.00 KiB	4	0xFF	BYTE
[T] - Extended Code Flash	0x1F000000	0x1F007FFF	32.00 KiB	512	0xFF	BYTE
[T] - Extended Code Flash	0x1F800000	0x1F807FFF	32.00 KiB	512	0xFF	BYTE
[C] - Checksum **(reserved virtual address)**	0x90300000	0x90300001	2 Byte	0	0xFF	BYTE
[M] - Metadata **(reserved virtual address)**	0x90500000	0x9050000B	12 Byte	0	0xFF	BYTE
[P] - eFUSE **(virtual address)**	0x90700000	0x907003FF	1.00 KiB	1	0x00	BYTE



	Memory Type	Start Address	End Address	Memory Size	Page Size	Blank Value	Address Unit
1	[F] - Main Flash	0x10000000	0x1082FFFF	8.19 MiB	512	0xFF	BYTE
2	[E] - Work Flash	0x14000000	0x1403FFFF	256.00 KiB	4	0xFF	BYTE
3	[S] - Supervisory Flash	0x17000000	0x17007FFF	32.00 KiB	512	0xFF	BYTE
4	[F] - Main Flash	0x18000000	0x1882FFFF	8.19 MiB	512	0xFF	BYTE
5	[E] - Work Flash	0x1C000000	0x1C03FFFF	256.00 KiB	4	0xFF	BYTE
6	[T] - Extended Code Flash	0x1F000000	0x1F007FFF	32.00 KiB	512	0xFF	BYTE
7	[T] - Extended Code Flash	0x1F800000	0x1F807FFF	32.00 KiB	512	0xFF	BYTE
8	[C] - Checksum (reserved virtual address)	0x90300000	0x90300001	2 Byte	0	0xFF	BYTE
9	[M] - Metadata (reserved virtual address)	0x90500000	0x9050000B	12 Byte	0	0xFF	BYTE
10	[P] - eFuse (virtual address)	0x90700000	0x907003FF	1.00 KiB	1	0x00	BYTE

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INFINEON TRAVEO2 eFUSE

This is an OTP area (One-Time-Programmable) and this means that once a bit is blown, so it has the '1' state, it cannot return to the '0' state.

Single eFUSE can be changed in state bit-by-bit by putting the value in .FRB file and using the program command.

Only bits that are different from '0' will be written because the original state of a bit of eFUSE is '0' and then can become '1' by blowing.
If an eFUSE byte (different from 0x0 and 0xFF) is on the FRB file but the target device has already that byte written, the eFUSE **is NOT blown another time**.

If an eFUSE byte (different from 0x0 and 0xFF) is on .FRB file but it is different from eFUSE byte read from device, only '1' bits will be written.

After programming (blowing process) a check operation (verify) checks byte-by-byte the eFUSE area, comparing .FRB eFUSE values with current device values read from eFUSE area.

The driver writes bit-by-bit the eFUSE value but the minimum blowing size is the value of **1 byte** in .FRB file, this means that in the .FRB you have to consider the entire 8-bit value of eFUSE.

Since the eFUSE area is not accessed via the address space then FlashRunner refers to a virtual address which is declared in the programming specification of Infineon. This address starts from 0x90700000 up to 0x907003FF and corresponds to the eFUSE **bit** area (**not byte area**).

According to specifications, each eFUSE byte is made up of 8 eFUSEs bits and each location of the virtual address space corresponds to the eFUSEs bit to be programmed.
Please see Infineon's programming specifications to better understand how eFUSE memory area works.

INFINEON TRAVEO2 Single Bank and Dual Bank

Traveo II has **Single Bank** and **Dual Bank** options.

In **Single Bank Mode** the Cortex core of the device has direct access to all the flash memory which is seen as a single continuous portion of the address space.
In other words, the flash is seen as a single block.

In **Dual Bank Mode** the memory is divided into two banks, which cannot be accessed directly and immediately because before the user has to select the bank to use.

For command specifications please refer to the `#TCSETPAR FLASH_BANK_MODE` or `#TCSETPAR WORKFLASH_BANK_MODE` description.

Once the bank has been selected, the user is allowed to program it.
Since the memory is not now a single block, the user has to use an FRB with half data and then the complete memory size.

The double bank option is a good way to introduce OTA updates because you can change the whole content of one bank.

Traveo II devices are very flexible thanks to the possibility of releasing OTA updates.
When you have to make an OTA update or in general firmware update of a microcontroller it means you want to rewrite a part of the flash.
The part you want to rewrite will have a new firmware which will be the one used as the main execution firmware.
However, it could happen that during the update the microcontroller turns off and corrupts the entire system.

To solve this problem, a second image (default image) is used, consisting of software that is used in the event of an emergency when the main updatable image has been corrupted.
Hence the need to execute, if necessary, a second image which serves to restore the first image.

NOTE: For further information refer to the document AN229058 on Infineon's website.

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INFINEON TRAVEO2 SWD and JTAG Locking

In Traveo II devices there is the possibility to lock permanently the DAP (Debug Access Port) of the SWD/JTAG.
This operation is irreversible and once the DAP is disabled, it is no longer possible to connect with the device.

To disable the DAP, it is necessary to set the **TOC2_FLAGS** which are 2 bytes located at the memory address **0x17007DF8** of the Supervisory Flash.

To lock the device, you can use the command `#TPCMD PATCH_SUPERVISORY_MEMORY`. Please refer to the command description.

Here are the **TOC2_FLAGS**:

Bit	Name	Description
bit [1:0]	**CLOCK_CONFIG**	Indicates clock frequency configuration. The clock should stay the same after Flash boot execution 0 = 8 MHz, IMO, no FLL 1 = 25 MHz IMO + FLL 2 = 50 MHz IMO + FLL 3 = Use ROM boot clock configuration
bit [4:2]	**LISTEN_WINDOW**	Determines the Listen window to allow sufficient time to acquire debug port. 0 = 20 ms (Default) 1 = 10 ms 2 = 1 ms 3 = 0 ms (No Listen window) 4 = 100 ms
bit [6:5]	**SWJ_PINS_CTL**	Determines if SWJ pins are configured in SWJ mode by Flash boot. 0 = Do not enable SWJ pins in Flash boot. Listen window is skipped 1 = Do not enable SWJ pins in Flash boot. Listen window is skipped 2 = Enable SWJ pins in Flash boot (default) 3 = Do not enable SWJ pins in Flash boot. Listen window is skipped
bit [8:7]	**APP_AUTH_CTL**	Determines if the application image digital signature verification (authentication) is performed: 0 = Authentication is enabled (default) 1 = Authentication is disabled 2 = Authentication is enabled (recommended) 3 = Authentication is enabled
bit [10:9]	**FB_BOOTLOADER_CTL**	Determine if the internal bootloader in Flash boot is disabled: 0 = Internal bootloader is disabled 1 = Internal bootloader is launched if the other bootloader conditions are met (default) 2 = Internal bootloader is disabled 3 = Internal bootloader is disabled.

Set **LISTEN_WINDOW** = **3** to disable the listening window of time to acquire the device in SWD or JTAG protocol.

Set **SWJ_PINS_CTL** = **0** to disable SWD or JTAG pin function (dedicated for debugging and flashing) after the Flash Boot has been executed.

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INFINEON TRAVEO2 Driver Parameters

The standard parameters are used to configure some specific options inside TRAVEO2 driver.

#TCSETPAR ENTRY_CLOCK

Syntax: **#TCSETPAR** ENTRY_CLOCK <Frequency>

<Frequency> Accepted parameters 4000000, 2000000, 1000000, 500000, 100000 Hz

Description: Set the JTAG/SWD frequency used in the Connect procedure before raising the PLL of the device, if the device PLL is available

Note: Default value 1.00 MHz

#TCSETPAR ACQUIRING_SEQUENCE

Syntax: **#TCSETPAR** ACQUIRING_SEQUENCE

Description: This parameter defines the entry mode
The acquiring chip procedures are defined by Infineon and you can find them in the Reference Manuals of Traveo II devices
The *ACQUIRE_CHIP* is a procedure that uses the reset line to establish the communication between the FlashRunner and the target device
The other procedure, *ALTERNATE_ACQUIRE_CHIP* does not use the reset line to establish the communication.

Note: By default, the driver uses the *ACQUIRE_CHIP* method

#TCSETPAR BLANKCHECK_IN_PROGRAM_FLASH

Syntax: **#TCSETPAR** BLANKCHECK_IN_PROGRAM_FLASH <Value>

<Value> Accepted values are Yes or No

Description: The blankcheck command can be executed on the Main Flash memory
There are two possible ways to perform the blankcheck operation
The first choice is to perform the command #TPCMD BLANKCHECK F
The second choice is to perform the operation during the #TPCMD PROGRAM F command

Note: None

#TCSETPAR BLANKCHECK_IN_PROGRAM_WFLASH

Syntax: **#TCSETPAR** BLANKCHECK_IN_PROGRAM_WFLASH <Value>

<Value> Accepted values are Yes or No

Description: The blankcheck command can be executed on the Work Flash memory
There are two possible ways to perform the blankcheck operation
The first choice is to perform the command #TPCMD BLANKCHECK E
The second choice is to perform the operation during the #TPCMD PROGRAM E command

Note: None

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#TCSETPAR EFUSE_MARGIN_LEVEL

Syntax: `#TCSETPAR EFUSE_MARGIN_LEVEL <NOMINAL_RESISTANCE|LOW_RESISTANCE|HIGH_RESISTANCE>`

NOMINAL_RESISTANCE → default read condition
LOW_RESISTANCE → -50% from nominal resistance
HIGH_RESISTANCE → +50% from nominal resistance

Description: This command is used to in order to define the Margin Verify mode for the eFUSE
The margin verify is available only for the eFUSE memory area
This verification procedure differs from the classic one in re-reading the values stored in the memory by changing certain levels of current and supply voltage of the flash memory
This allows greater reliability as the data are read back in power range conditions other than the typical ones
The procedure provided by Infineon is carried out automatically by the HW of the device during the writing

Note: All other information regarding this command is **Under NDA**

#TCSETPAR FLASH_BANK_MODE

Syntax: `#TCSETPAR FLASH_BANK_MODE <SINGLE_BANK|DUAL_BANK_MAPPING_A|DUAL_BANK_MAPPING_B>`

Description: This command enables the dual bank mode if you select the DUAL_BANK_MAPPING_A or B parameter

The Main Flash memory area supports the dual bank mode and when this option is selected the flash memory region is split into two half banks

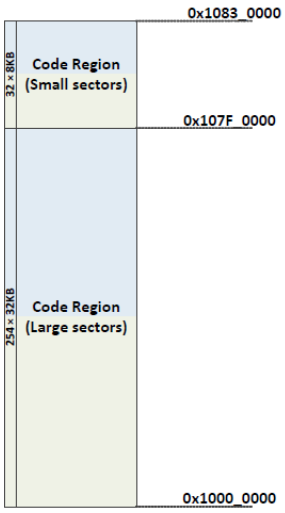
One is called Logical Bank 0 and the other is called Logical Bank 1

On the below chapter Single Bank and Dual Bank Overview there is an explanation of the dual bank mode application

DUAL_BANK_MAPPING_A

The data to be programmed have to be half the total size of the Main Flash.

For this example, we have to program data from 0x10000000 to 0x103F7FFF (for the large sectors) and from 0x103F8000 to 0x10417FFF.
Following this example, the memory programmed will be the green one:



DUAL_BANK_MAPPING_B

The data to be programmed have to be half the total size of the Main Flash.

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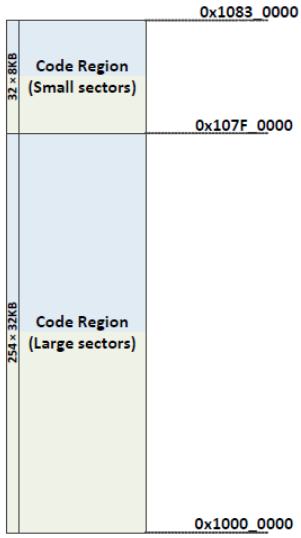
For this example, we have to program data from 0x10000000 to 0x103F7FFF (for the large sectors) and from 0x103F8000 to 0x10417FFF.
Following this example, the memory programmed will be the blue one:



DUAL_BANK_MAPPING_BOTH_A_AND_B

The data to be programmed have to be half the total size of the Main Flash.

For this example, we have to program data from 0x10000000 to 0x103F7FFF (for the large sectors) and from 0x103F8000 to 0x10417FFF.

Following this example, the memory programmed will be both green and blue.
The difference from a normal program is that the green part will contain the original data and the blue part will contain an exact copy.

#TCSETPAR WORKFLASH_BANK_MODE

Syntax: `#TCSETPAR WORKFLASH_BANK_MODE <SINGLE_BANK|DUAL_BANK_MAPPING_A|DUAL_BANK_MAPPING_B>`

Description: This command enables the dual bank mode if you select the DUAL_BANK_MAPPING_A or B parameter

The Work Flash memory area supports the dual bank mode and when this option is selected the flash memory region is split into two half banks

One is called Logical Bank 0 and the other is called Logical Bank 1

In the below chapter Single Bank and Dual Bank Overview there is an explanation of the dual bank mode application

DUAL_BANK_MAPPING_A

The data to be programmed have to be half the total size of the Work Flash.

For this example, we have to program data from 0x14000000 to 0x1400BFFF (for the large sectors) and from 0x1400C000 to 0x14010000.
Following this example, the memory programmed will be the green one:

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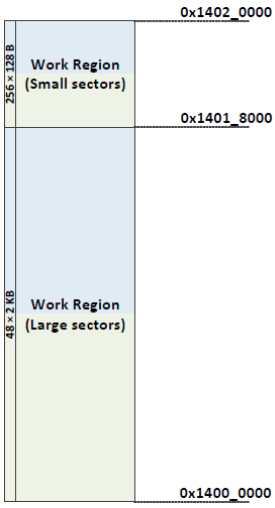
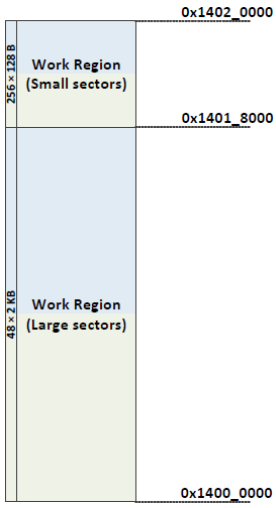


DUAL_BANK_MAPPING_B

The data to be programmed have to be half the total size of the Work Flash.

For this example, we have to program data from 0x14000000 to 0x1400BFFF (for the large sectors) and from 0x1400C000 to 0x14010000.
Following this example, the memory programmed will be the blue one:



DUAL_BANK_MAPPING_BOTH_A_AND_B

The data to be programmed have to be half the total size of the Work Flash.

For this example, we have to program data from 0x14000000 to 0x1400BFFF (for the large sectors) and from 0x1400C000 to 0x14010000.
Following this example, the memory programmed will be the both the green and the blue.

The difference from a normal program is that the green part will contain the original data and the blue part will contain an exact copy.

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#TCSETPAR SAMPLING_POINT

Syntax: `#TCSETPAR SAMPLING_POINT <Value>`

`<Value>` Accepted values are in the range 1-15

Description: Use this parameter to permanently set the sampling point of the FPGA
It is recommended to leave this parameter with the default value

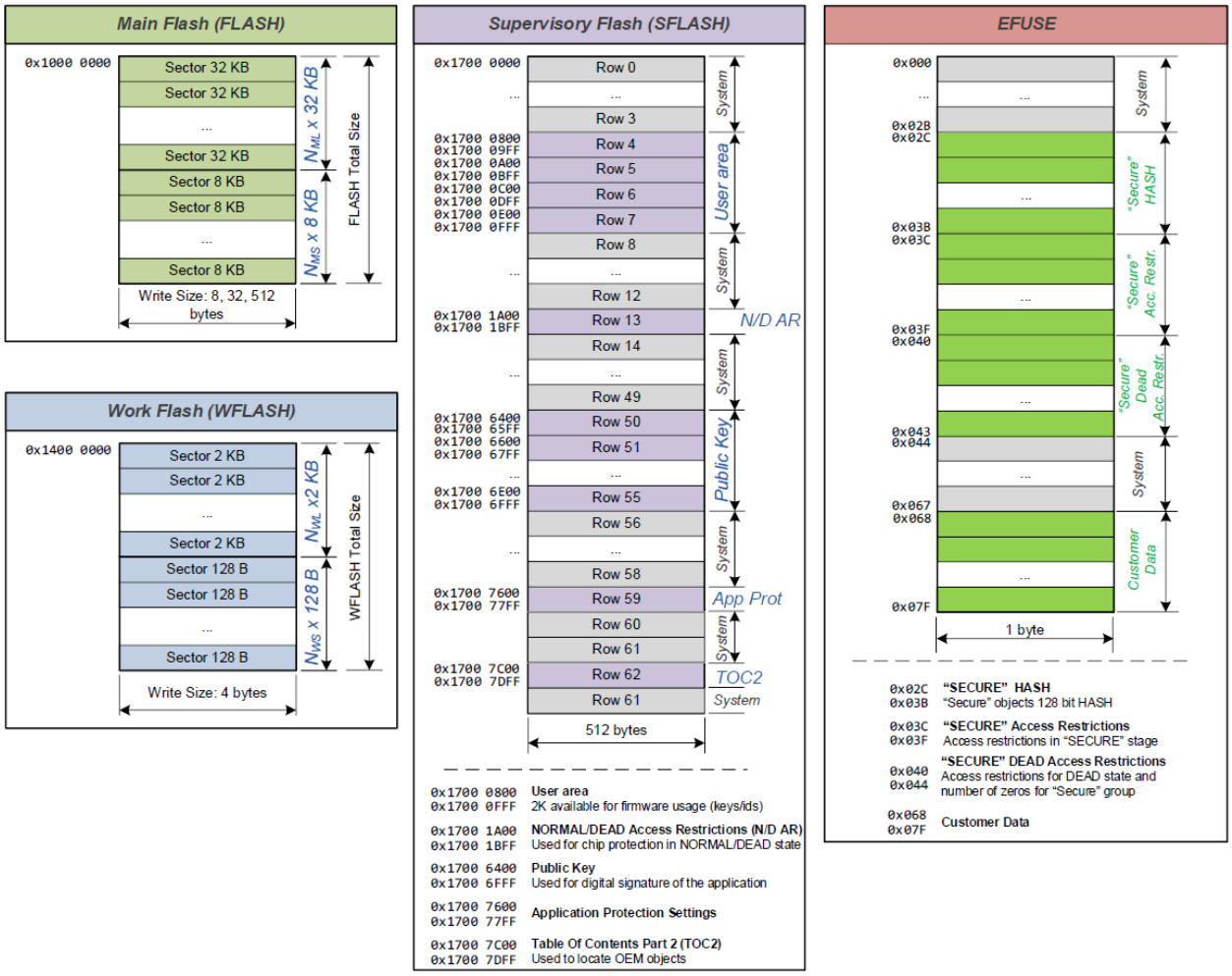
Note: Default value 17

INFINEON TRAVEO2 Driver Commands

Here you can find the complete list of all available commands for TRAVEO2 driver.

```
F → Main Flash
E → Work Flash
S → Supervisory Flash
T → Extended Code Flash
C → Checksum (reserved virtual address) On this virtual memory area is stored the checksum of the firmware
M → Metadata (reserved virtual address) On this virtual memory area is stored the Silicon ID and other relevant data
P → eFUSE (virtual address)
X → External Memory (Hyperflash memory or generic external memory connected to Traveo II device)
```

Traveo 2 devices with one Flash Controller:



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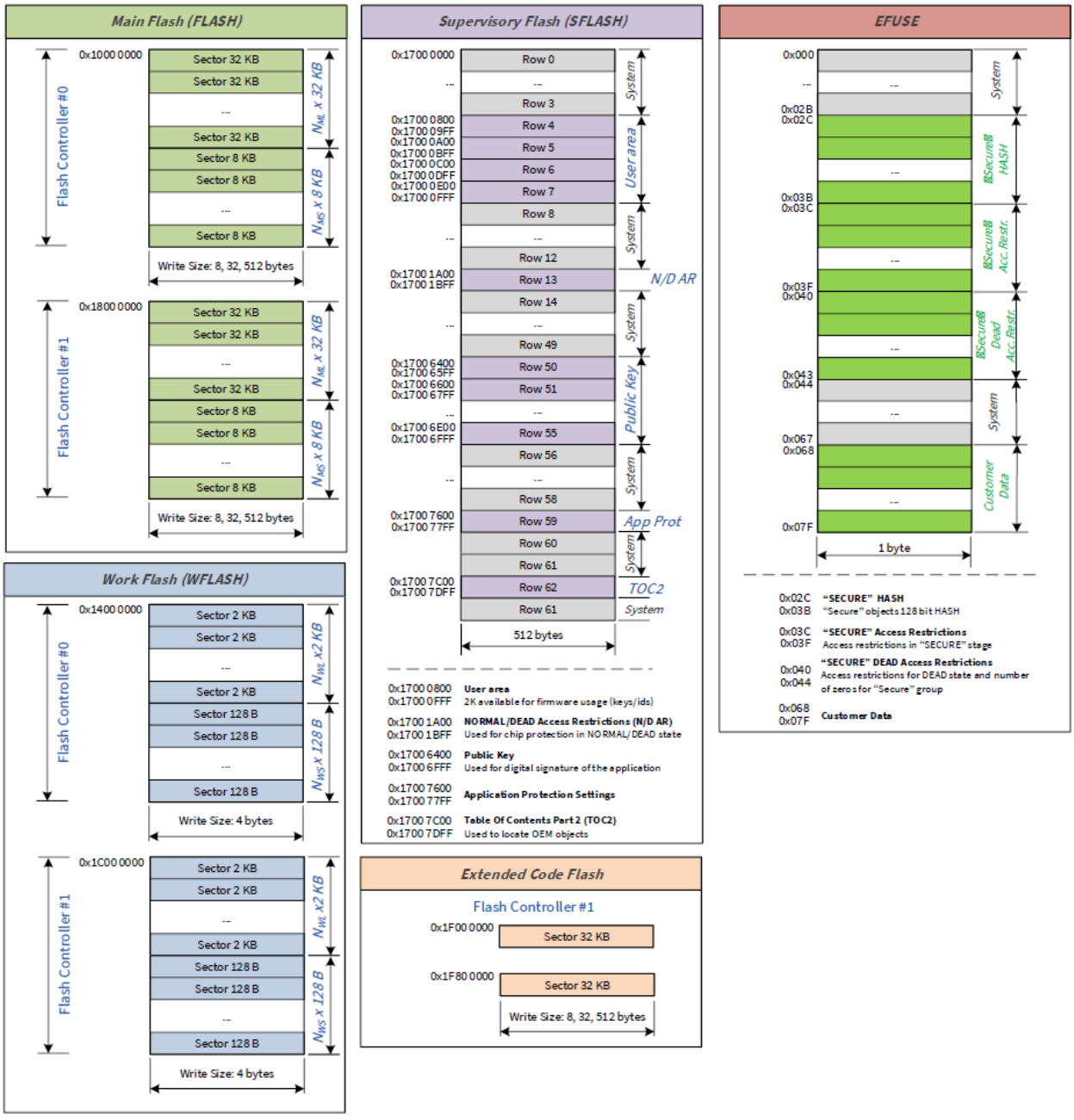
Traveo 2 devices with two Flash Controller:



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#TPCMD CONNECT

#TPCMD CONNECT

This function performs the entry and is the first command to be executed when starting the communication with the device.
There are two types of connect, regarding this please read **#TCSETPAR** ACQUIRING SEQUENCE.
Here you see can the log of a standard connect with the Acquire Chip procedure selected:

Connect procedure when the device is blank:

```
---#TPCMD CONNECT
Protocol selected SWD.
Toggling XRES pin to execute Acquire Chip procedure.
ID-Code read correctly at 4.00 MHz after 49 retries.
JTAG-SWD Debug Port enabled.
Move Traveo II internal state to Test Mode.
Traveo II enter into Test Mode.
Scanning AP map to find all APs:
 * AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[1] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[2] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[3] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[4] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[5] IDR: 0x84770001, Type: AMBA AHB3 bus.
Scanning AP to find all cores:
 * AP[1] ARM - CPUID: 0x410CC601 - Found Cortex M0+ revision r0p1.
 * AP[2] ARM - CPUID: 0x411FC272 - Found Cortex M7 revision r1p2.
 * AP[3] ARM - CPUID: 0x411FC272 - Found Cortex M7 revision r1p2.
 * AP[4] ARM - CPUID: 0x411FC272 - Found Cortex M7 revision r1p2.
 * AP[5] ARM - CPUID: 0x411FC272 - Found Cortex M7 revision r1p2.
Try to halt the Cortex M0+ core:
 * AP[1] Cortex M0+ core halted after 0.002 s.
 * AP[1] Cortex M0+ core Program Counter is 0x000003D2.
Try to halt the Cortex M7 core:
 * AP[2] Cortex M7 core halted after 0.001 s.
 * AP[1] Cortex M0+ core Program Counter is 0x0000020A.
Try to halt the Cortex M7 core:
 * AP[3] Cortex M7 core halted after 0.002 s.
 * AP[1] Cortex M0+ core Program Counter is 0x00000214.
Try to halt the Cortex M7 core:
 * AP[4] Cortex M7 core halted after 0.001 s.
 * AP[1] Cortex M0+ core Program Counter is 0x0000024E.
Try to halt the Cortex M7 core:
 * AP[5] Cortex M7 core halted after 0.001 s.
 * AP[1] Cortex M0+ core Program Counter is 0x00000258.
Try to execute the Acquire Chip method procedure:
 * AP[1] Cortex M0+ core Program Counter is 0x000003D2.
 * AP[1] Cortex M0+ core Vector Table base 0xFFFF0000.
 * Vector Table value means that the Flash is empty or TOC is corrupted.
> Acquire Chip method procedure completed.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 4 [Range 4-7].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Read device informations:
 * FamilyId: 0x0114.
 * Revision: 0x11.
 * SiliconID: 0xED04.
 * Protect state: 0x2: Virgin - [NORMAL] - Secure - Dead.
 * Life cycle stage: 0x7 - Normal Provisioned.
 * Flash boot version: 0xA301.
 * SROM firmware version: 0x0801.
Read device unique ID:
 * Unique ID0: 0x008D24EC, Unique ID1: 0xFF0A0504, Unique ID2: 0x7C090600.
Normal device access restrictions:
 * Enabled Cortex M0-AP access.
 * Enabled Cortex CM7 n.0/CM7 n.1 AP access.
```


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```
 * Enabled system AP access.
 * MPU is locked, all SRAM is accessible.
 * Enabled Direct Execute system call functionality.
 * Entire Flash main region is accessible.
 * Entire SRAM main region is accessible.
 * Entire Work Flash main region is accessible.
 * Entire Supervisory Flash main region is accessible.
> Check Traveo II Silicon ID passed from SMH database [0xED04].
* Check Traveo II Silicon ID from source file not available.
Time for Connect: 0.509 s.
>|
```

Connect procedure when the device is already programmed:

```
---#TPCMD CONNECT
Protocol selected SWD.
Toggling XRES pin to execute Acquire Chip procedure.
ID-Code read correctly at 4.00 MHz after 161 retries.
JTAG-SWD Debug Port enabled.
Move Traveo II internal state to Test Mode.
Traveo II enter into Test Mode.
Scanning AP map to find all APs:
 * AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[1] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[2] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[3] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[4] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[5] IDR: 0x84770001, Type: AMBA AHB3 bus.
Scanning AP to find all cores:
 * AP[1] ARM - CPUID: 0x410CC601 - Found Cortex M0+ revision r0p1.
 * AP[2] ARM - CPUID: 0x411FC272 - Found Cortex M7 revision r1p2.
 * AP[3] ARM - CPUID: 0x411FC272 - Found Cortex M7 revision r1p2.
 * AP[4] ARM - CPUID: 0x411FC272 - Found Cortex M7 revision r1p2.
 * AP[5] ARM - CPUID: 0x411FC272 - Found Cortex M7 revision r1p2.
Try to halt the Cortex M0+ core:
 * AP[1] Cortex M0+ core halted after 0.001 s.
 * AP[1] Cortex M0+ core Program Counter is 0x000003D2.
Try to halt the Cortex M7 core:
 * AP[2] Cortex M7 core halted after 0.001 s.
 * AP[1] Cortex M0+ core Program Counter is 0x000001F6.
Try to halt the Cortex M7 core:
 * AP[3] Cortex M7 core halted after 0.001 s.
 * AP[1] Cortex M0+ core Program Counter is 0x0000022C.
Try to halt the Cortex M7 core:
 * AP[4] Cortex M7 core halted after 0.001 s.
 * AP[1] Cortex M0+ core Program Counter is 0x0000024A.
Try to halt the Cortex M7 core:
 * AP[5] Cortex M7 core halted after 0.002 s.
 * AP[1] Cortex M0+ core Program Counter is 0x00000256.
Try to execute the Acquire Chip method procedure:
 * AP[1] Cortex M0+ core Program Counter is 0x000003D2.
 * AP[1] Cortex M0+ core Vector Table base 0x10000100.
 * AP[1] Cortex M0+ core Reset Address 0x10006CF5.
 * Set specific hardware breakpoint 0xD0006CF5.
 * Trigger a software reset to restart CPU.
 * Reconnect and waiting for CPU to hit the breakpoint.
 * AP[1] Cortex M0+ core Program Counter is 0x10006CF4.
> Acquire Chip method procedure completed.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 4 [Range 4-7].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Read device informations:
 * FamilyId: 0x0114.
 * Revision: 0x11.
 * SiliconID: 0xED04.
 * Protect state: 0x2: Virgin - [NORMAL] - Secure - Dead.
```


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```
 * Life cycle stage: 0x7 - Normal Provisioned.
 * Flash boot version: 0xA301.
 * SROM firmware version: 0x0801.
Read device unique ID:
 * Unique ID0: 0x008D24EC, Unique ID1: 0xFF0A0504, Unique ID2: 0x7C090600.
Normal device access restrictions:
 * Enabled Cortex M0-AP access.
 * Enabled Cortex CM7 n.0/CM7 n.1 AP access.
 * Enabled system AP access.
 * MPU is locked, all SRAM is accessible.
 * Enabled Direct Execute system call functionality.
 * Entire Flash main region is accessible.
 * Entire SRAM main region is accessible.
 * Entire Work Flash main region is accessible.
 * Entire Supervisory Flash main region is accessible.
> Check Traveo II Silicon ID passed from SMH database [0xED04].
* Check Traveo II Silicon ID from source file not available.
Time for Connect: 0.532 s.
>|
```

ID-Code read correctly at 1.00 MHz after 12 retries

This is normal behavior because when the Traveo2 device is powered on the SWD/JTAG port is not immediately available.
The TRAVEO2 driver tries to read the ID code several times before the SWD/JTAG port is activated.

Check Traveo II Silicon ID from source file not available

This warning means that the FRB file is not present or the Silicon ID is not available inside FRB file.
Therefore, it is not possible to compare the Silicon ID read from the device with the one present in the file to be programmed.

#TPCMD MASSERASE

#TPCMD MASSERASE <F|E|X>
This function performs a masserase for Main Flash, Work Flash or External Memory.

#TPCMD ERASE

#TPCMD ERASE <F|E|X> <start address> <size>
This function performs a sector erase for the Main Flash, Work Flash or External Memory.
Main Flash has several large 32KiB sectors and several small 16KiB sectors.
The Work Flash has several large 2 KiB sectors and several small 128 B sectors.
The driver automatically handles the erase of large and/or small sectors depending on the address and size inserted.
In addition to this, the driver handles the alignment of Start address and Size if the inputs are not aligned to the memory granularity.

#TPCMD BLANKCHECK

#TPCMD BLANKCHECK <F|E|X>
Blankcheck is only available for Main Flash, Work Flash and External Memory.
Verify if all memory is erased.

#TPCMD BLANKCHECK <F|E|X> <start address> <size>
Blankcheck is only available for Main Flash, Work Flash and External Memory.
Verify if selected part of memory is erased.
Enter the Start Address and Size in hexadecimal format.

#TPCMD PROGRAM

#TPCMD PROGRAM <F|E|S|P|X>

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Program available for Main Flash, Work Flash, Supervisory Flash, eFUSE and External Memory.
Programs all memory of the selected type based on the data in the FRB file.

The Supervisory Flash contains bytes whose value corresponds to the Traveo2 settings and protections.
Writing random values in this area produces unpredictable results, so if you need to modify only some specific bits, please use the `#TPCMD PATCH_SUPERVISORY_FLASH` command.

The eFUSE is an OTP area (One-Time-Programmable) and once a byte is written it cannot be changed anymore.
Note that both Supervisory Flash and eFUSE have zones that cannot be programmed.

`#TPCMD PROGRAM <F|E|S|P|X> <start address> <size>`
Program available for Main Flash, Work Flash, Supervisory Flash, eFUSE and External Memory.
Programs selected part of memory of the selected type based on the data in the FRB file.
Enter the Start Address and Size in hexadecimal format.

The Supervisory Flash contains bytes whose value corresponds to the Traveo2 settings and protections.
Writing random values in this area produces unpredictable results, so if you need to modify only some specific bits, please use the `#TPCMD PATCH_SUPERVISORY_FLASH` command.

The eFUSE is an OTP area (One-Time-Programmable) and once a byte is written it cannot be changed anymore.
Note that both Supervisory Flash and eFUSE have zones that cannot be programmed.

#TPCMD VERIFY

`#TPCMD VERIFY <F|E|S|P> <R>`
R: Readout Mode.
Verify Readout available for Main Flash, Work Flash, Supervisory Flash and eFUSE.
Verify all memory of the selected type based on the data in the FRB file.

`#TPCMD VERIFY <F|E|S|P> <R> <start address> <size>`
R: Readout Mode.
Verify Readout available for Main Flash, Work Flash, Supervisory Flash and eFUSE.
Verify selected part of memory of the selected type based on the data in the FRB file.
Enter the Start Address and Size in hexadecimal format.

`#TPCMD VERIFY <F|E|S|P> <S>`
S: Checksum 32 Bit Mode.
Verify Checksum available for Main Flash, Work Flash, Supervisory Flash and eFUSE.
Verify all memory of the selected type based on the data in the FRB file.

`#TPCMD VERIFY <F|E|S|P> <S> <start address> <size>`
S: Checksum 32 Bit Mode.
Verify Checksum available for Main Flash, Work Flash, Supervisory Flash and eFUSE.
Verify selected part of memory based on the data in the FRB file.
Enter the Start Address and Size in hexadecimal format.

#TPCMD VERIFY_MARGIN_EFUSE

`#TPCMD MARGIN_VERIFY`
Margin Verify is available only for eFUSE memory.
Verify Margin of all eFUSEs.

`#TPCMD MARGIN_VERIFY <Virtual Start Address> <Virtual Size>`
Margin Verify is available only for eFUSE memory.
Verify Margin selected part of eFUSEs.

#TPCMD READ

`#TPCMD READ <F|E|S|P|X>`
`#TPCMD READ <F|E|S|P|X> <start address> <size>`

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Read function for Main Flash, Work Flash, Supervisory Flash, eFUSE or External Memory.
The result of the read command will be visible into the Terminal.

Note that some eFUSE bytes cannot be read for protection reasons.

Regarding the Work Flash Memory, when it is not programmed, if a reading operation occurs, an ECC error is generated.
This means that Work Flash memory cannot be read when it is not programmed.

To overcome this problem, a blankcheck is performed before reading the memory via a specific API internal to the Traveo II.
If the memory is blank at that specific address, then in the terminal you will see "????".

Here an example of this behaviour:

```
> 02|Read[0x1400FF90]: 0x5D 0x08 0xCC 0x12 0x63 0x90 0x0E 0x1E | 0x03 0xF4 0x7E 0xA5 0x16 0xC5 0x5D 0xDC
> 02|Read[0x1400FFA0]: 0xCF 0xCE 0x70 0x44 0x07 0x8C 0xFB 0x35 | 0x02 0xDF 0xF7 0x26 0x1A 0x65 0x78 0x51
> 02|Read[0x1400FFB0]: 0x1B 0x26 0xC8 0x75 0x3D 0x81 0xAB 0xC6 | 0x0C 0x83 0xC9 0x59 0xA5 0x14 0x46 0x8F
> 02|Read[0x1400FFC0]: 0x0D 0xAD 0xED 0x57 0xA6 0x76 0x83 0x4D | 0xF0 0x01 0x28 0xFD 0x16 0x13 0xD7 0xE2
> 02|Read[0x1400FFD0]: 0x11 0x16 0x6A 0xE0 0x3F 0x31 0xBA 0x53 | 0xD1 0x2A 0xB3 0xEC 0x63 0x7E 0x82 0x00
> 02|Read[0x1400FFE0]: 0xA0 0x5B 0x2F 0xFD 0xCE 0x70 0x46 0x26 | 0x99 0xAF 0x67 0xCF 0x7F 0x7B 0xD9 0xB8
> 02|Read[0x1400FFF0]: 0xB1 0xEE 0x80 0x3D 0x54 0x10 0xCE 0x82 | 0x6B 0x4D 0x8B 0xCB 0xD3 0x6E 0x94 0xA2
> 02|Read[0x14010000]: ???? ???? ???? ???? ???? ???? ???? ???? | ???? ???? ???? ???? ???? ???? ???? ????
> 02|Read[0x14010010]: ???? ???? ???? ???? ???? ???? ???? ???? | ???? ???? ???? ???? ???? ???? ???? ????
> 02|Read[0x14010020]: ???? ???? ???? ???? ???? ???? ???? ???? | ???? ???? ???? ???? ???? ???? ???? ????
> 02|Read[0x14010030]: ???? ???? ???? ???? ???? ???? ???? ???? | ???? ???? ???? ???? ???? ???? ???? ????
> 02|Read[0x14010040]: ???? ???? ???? ???? ???? ???? ???? ???? | ???? ???? ???? ???? ???? ???? ???? ????
> 02|Read[0x14010050]: ???? ???? ???? ???? ???? ???? ???? ???? | ???? ???? ???? ???? ???? ???? ???? ????
> 02|Read[0x14010060]: ???? ???? ???? ???? ???? ???? ???? ???? | ???? ???? ???? ???? ???? ???? ???? ????
> 02|Read[0x14010070]: ???? ???? ???? ???? ???? ???? ???? ???? | ???? ???? ???? ???? ???? ???? ???? ????
```

#TPCMD DUMP

```
#TPCMD DUMP <F|E|S|P|X>
#TPCMD DUMP <F|E|S|P|X> <start address> <size>
```

Dump command for the Main Flash, Supervisory Flash, eFUSE or External Memory.
The result of the dump command will be stored in the FlashRunner 2.0 internal memory.

As for the read command, some eFUSE bytes cannot be dumped.
The Work Flash cannot be dumped if it is not programmed because we cannot put the "????" inside a .bin file when the selected address of Work Flash memory is blank

#TPCMD GET_UNIQUE_ID

Syntax: `#TPCMD GET_UNIQUE_ID`

Prerequisites: none

Description: This function reads the unique ID of the device
The result of this command will be printed on the Real Time Log and on the Terminal

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD GET_UNIQUE_ID
Read device unique ID:
 * Unique ID0: 0x00899EB4, Unique ID1: 0xFF083D0F, Unique ID2: 0x78081C00.
Time for Get Unique ID: 0.001 s.
```

#TPCMD GET_DEVICE_INFORMATIONS

Syntax: `#TPCMD GET_DEVICE_INFORMATIONS`

Prerequisites: none

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Description: This function gets the device information as the family, unique ID and more

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD GET_DEVICE_INFORMATIONS
Read device informations:
 * FamilyId: 0x0104.
 * Revision: 0x13.
 * SiliconID: 0xE6C9.
 * Protect state: 0x2: Virgin - [NORMAL] - Secure - Dead.
 * Life cycle stage: 0x7 - Normal Provisioned.
 * Flash boot version: 0xA301.
 * SROM firmware version: 0x0601.
Read device unique ID:
 * Unique ID0: 0x00899EB4, Unique ID1: 0xFF083D0F, Unique ID2: 0x78081C00.
Normal device access restrictions:
 * Enabled Cortex M0-AP access.
 * Enabled Cortex M4 AP access.
 * Enabled system AP access.
 * MPU is locked, all SRAM is accessible.
 * Enabled Direct Execute system call functionality.
 * Entire Flash main region is accessible.
 * Entire SRAM main region is accessible.
 * Entire Work Flash main region is accessible.
 * Entire Supervisory Flash main region is accessible.
Time for Get Device Informations: 0.002 s.
```

#TPCMD OVERVIEW_SUPERVISORY_FLASH

Syntax: `#TPCMD OVERVIEW_SUPERVISORY_FLASH`

Prerequisites: none

Description: This command reads the Supervisory Flash printing its content on the Workbench Real Time Log. Here below there is a little extract of the result of the command execution.

> *Supervisory Flash - Table of Contents Part 2 (TOC2), used to locate OEM objects:*
> *Address 0x17007C00: FC010000 20122101 00000000 00000010 00000000 00000000 etc ...*
>
> *The data has to be read in this way:*
> *most significant byte 0x00 then 0x00 then 0x01 and then, the less significant byte is 0xFC.*
> *If you want to reprogram this value the right data value is 0x000001FC*

#TPCMD OVERVIEW_SUPERVISORY_FLASH_NADR

Syntax: `#TPCMD OVERVIEW_SUPERVISORY_FLASH_NADR`

Prerequisites: none

Description: This command analyses the NADR (Normal/Dead Device Access Restrictions) located into the Supervisory Flash

Examples: Correct command execution: 😊

```
---#TPCMD OVERVIEW_SUPERVISORY_FLASH_NADR
Analyze NADR located into Supervisory Flash:
Normal device access restrictions:
 * Enabled Cortex M0-AP access.
 * Enabled Cortex M4 AP access.
 * Enabled system AP access.
 * MPU is locked, all SRAM is accessible.
 * Enabled Direct Execute system call functionality.
 * Entire Flash main region is accessible.
 * Entire SRAM main region is accessible.
 * Entire Work Flash main region is accessible.
 * Entire Supervisory Flash main region is accessible.
```


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```
Dead device access restrictions:
 * Enabled Cortex M0-AP access.
 * Enabled Cortex M4 AP access.
 * Enabled system AP access.
 * MPU is locked, all SRAM is accessible.
 * Disabled Direct Execute system call functionality.
 * Entire Flash main region is accessible.
 * Entire SRAM main region is accessible.
 * Entire Work Flash main region is accessible.
 * Entire Supervisory Flash main region is accessible.
Time for Read Mem: 0.002 s
```

#TPCMD OVERVIEW_SUPERVISORY_FLASH_SWPU

Syntax: **#TPCMD** OVERVIEW_SUPERVISORY_FLASH_SWPU

Prerequisites: none

Description: This command analyses the SWPU, FWPU, ERPU and EWPU located into the Supervisory Flash
SWPU is used to implement access restrictions to Main Flash (program/erase) and eFUSE (read/write)

Examples: Correct command execution: 😊

```
---#TPCMD OVERVIEW_SUPERVISORY_FLASH_SWPU
Analyze SWPU located into Supervisory Flash:
 * Found valid object size of 48 bytes.
 * Get the number of FWPU (Flash Write Protection Unit) object:
   * Found 0 FWPU object.
 * Get the number of ERPU (eFuse Read Protection Unit) object:
   * Found 1 ERPU object.
     * Analyze ERPU object n 1.
       * Address:        0x00000068.
       * Size:           0x80000018.
       * SL attributes:  0x00FF0007.
       * MS attributes:  0x00FF0007.
 * Get the number of EWPU (eFuse Write Protection Unit) object:
   * Found 1 EWPU object.
     * Analyze EWPU object n 1.
       * Address:        0x00000068.
       * Size:           0x80000018.
       * SL attributes:  0x00FF0007.
       * MS attributes:  0x00FF0007.
Value for PU OBJECT SIZE is correct.
Time for Overview Supervisory Flash SWPU: 0.003 s.
```

#TPCMD OVERVIEW_SUPERVISORY_FLASH_TOC2

Syntax: **#TPCMD** OVERVIEW_SUPERVISORY_FLASH_TOC2

Prerequisites: none

Description: This command analyses the TOC2 located into the Supervisory Flash

Examples: Correct command execution: 😊

```
---#TPCMD OVERVIEW_SUPERVISORY_FLASH_TOC2
Analyze TOC2 located into Supervisory Flash:
 * Object size in bytes for CRC calculation starting from offset 0x00: 0x000001FC.
 * Magic number: 0x01211220.
 * Null-terminated table of pointers representing the SMIF configuration structure: 0x00000000.
 * Address of First User Application Object: 0x10000000.
 * Format of First User Application Object: 0x00000000 - Basic.
 * Address of Second User Application Object: 0x00000000.
 * Format of Second User Application Object: 0x00000000 - Basic.
 * Address of First CM4 or CM7 core1 User Application Object: 0x00000000.
 * Address of Second CM4 or CM7 core1 User Application Object: 0x00000000.
 * Address of First CM4 or CM7 core2 User Application Object: 0x00000000.
 * Address of Second CM4 or CM7 core2 User Application Object: 0x00000000.
 * Number of additional objects to be verified for SECURE_HASH: 0x00000003.
 * Address of signature verification key: 0x00000000.
 * Address of Application Protection: 0x17007600.
```


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```
  * TOC2 Revision: 0x00000000.
  * Controls default configuration: 0x00000242.
    * Clock frequency configuration: 50MHz, IMO + FLL (default).
    * Listen window to allow sufficient time to acquire debug port: 20 ms (default).
    * SWJ pins configuration: Enable SWJ pins in Flash boot (default).
    * Image digital signature verification: Authentication is enabled.
    * Internal bootloader in flash boot: Internal bootloader is launched if other bootloader
conditions are met (default).
Time for Overview Supervisory Flash TOC2: 0.003 s.
```

#TPCMD GENERATE_HASH

Syntax: `#TPCMD GENERATE_HASH <FACTORY_HASH|ALL_OBJECTS>`

FACTORY_HASH → Generates the factory hash
ALL_OBJECTS → Generates the hash of all objects according to TOC1 and TOC2 tables

Prerequisites: none

Description: This command returns the truncated SHA-256 of the Flash boot programmed in the Supervisory Flash
Please refer to specific Reference Manual of your Traveo II device to have full description of how this command works

#TPCMD CHECK_FACTORY_HASH

Syntax: `#TPCMD CHECK_FACTORY_HASH`

Prerequisites: none

Description: This command generates the factory hash according to TOC1 table and compares with the FACTORY1_HASH fuses
Please refer to specific Reference Manual of your Traveo II device to have full description of how this command works

#TPCMD COMPUTE_BASIC_HASH

Syntax: `#TPCMD COMPUTE_BASIC_HASH <BASIC|CRC8SAE> <Start address> <Size Bytes>`

Prerequisites: none

Description: This command generates the hash of the flash region provided as input.
The command allows to select between BASIC (Basic Hash) or CRC8SAE.
The Size Bytes parameter must be grater or equal to 1
Please refer to specific Reference Manual of your Traveo II device to have full description of how this command works

Examples: Correct command execution: 😊

Example with BASIC parameter:

```
---#TPCMD COMPUTE_BASIC_HASH BASIC 0x10000000 0x10
Compute basic Hash:
 * Data Hash: 0x38.
Time for Compute BASIC Hash: 0.001 s.
```

Example with CRC8SAE parameter:

```
---#TPCMD COMPUTE_BASIC_HASH CRC8SAE 0x10000000 0x10
Compute CRC8SAE Hash:
 * Data Hash: 0xE9.
Time for Compute CRC8SAE Hash: 0.001 s.
```


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#TPCMD COMPUTE_CHECKSUM

Syntax: `#TPCMD COMPUTE_CHECKSUM <FLASH|WORK_FLASH|SUPERVISORY_FLASH> <BANK0|BANK1> <PAGE|WHOLE_MEMORY> <Row ID>`

Prerequisites: none

Description: This command returns the sum of each byte read.
The Row ID parameter is needed only if the previous parameter is PAGE.
Please refer to specific Reference Manual of your Traveo II device to have full description of how this command works

#TPCMD PATCH_SUPERVISORY_MEMORY

Syntax: `#TPCMD PATCH_SUPERVISORY_MEMORY <Address> <Value> <Mask>`

Prerequisites: none

Description: This command allows the user to patch some specific data at a certain address (into the Supervisory Flash) without erasing the other addresses
Here below there are some examples:

1. `#TPCMD PATCH_SUPERVISORY_MEMORY 0x17007C00 0x12345678 0x00000000`

   This command does not program the value 0x12345678 because the mask is all 0x00000000 and for this reason the value will not be programmed at that address.

   More precisely we read all the data aligned to 512 bytes and we patch the data at 0x17007C00 with the value inserted by the user only if the corresponding bit is equal to 1 in the mask field.

   For example, if you set the mask equal to 0x0000000F you change only the bits where the mask is 1 and the other bits will not change.

2. `#TPCMD PATCH_SUPERVISORY_MEMORY 0x17007C00 0x000001FC 0xFFFFFFFF`

   This command allows to program the value 0x000001FC at the address 0x17007C00 without considering the memory content at this address because the mask is all 1.

   Here some examples with custom mask:

   This is the memory content using the command `#TPCMD OVERVIEW_SUPERVISORY_FLASH`:

   Address 0x17000800: BBAA00FF FFFFFFFF FFFFFFFF FFFFFFFF

   If for example you want to change only the first byte at the address 0x17000800 (the first byte is 0xBB) with a new value like 0xCC, you must use the following syntax:

3. `#TPCMD PATCH_SUPERVISORY_MEMORY 0x17000800 0x000000CC 0x000000FF`

   In this case using the mask with only the first byte with all bits at 1 you change only the first byte of the memory to 0xCC and the rest will be untouched.

   In fact, if you execute another time the command `#TPCMD OVERVIEW_SUPERVISORY_FLASH` you can see that:

   Address 0x17000800: CCAA00FF FFFFFFFF FFFFFFFF FFFFFFFF

   Now if for example you want to change another address like 0x17000808 using the command

   `#TPCMD PATCH_SUPERVISORY_MEMEORY` 0x17000808 0xADDEADDE 0xFFFFFFFF

   You can see the new content of the memory

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Address 0x17000800: CCAA00FF FFFFFFFF DEADDEAD FFFFFFFF

As you can see the previous address has been left as it was before.

#TPCMD CONFIGURE_REGULATOR

Syntax: `#TPCMD CONFIGURE_REGULATOR <PMIC|TRANSISTOR> <ENABLE_POLARITY_HIGH|ENABLE_POLARITY_LOW> <RESET_POLARITY_HIGH|RESET_POLARITY_LOW> <HC_REG_NORMAL_MODE|HC_REG_DEEPSLEEP_MODE> <USE_LINEAR_REGULATOR|NO_LINEAR_REGULATOR> <USE_RADJ|NO_RADJ> <GENERATE_VADJ|NOT_GENERATE_VADJ> <RADJ Value> <Wait Counts>`

Prerequisites: none

Description: This command is used to configure the high-current regulator (REGHC) for devices that include REGHC, or PMIC for devices that use PMIC control without REGHC.
Please refer to specific Reference Manual of your Traveo II device to have full description of how this command works:

#TPCMD SWITCH_OVER_REGULATORS

Syntax: `#TPCMD SWITCH_OVER_REGULATORS <PMIC|TRANSISTOR> <SWITCH_TO_LINEAR_REGULATOR|SWITCH_TO_REGHC>`

Prerequisites: none

Description: This command is used to switch between the high-current regulator (REGHC or PMIC without REGHC) required to run CM7 and the linear regulator (LDO)
Please refer to specific Reference Manual of your Traveo II device to have full description of how this command works

#TPCMD LOAD_REGULATOR_TRIMS

Syntax: `#TPCMD LOAD_REGULATOR_TRIMS <REGHC|LDO> <FORCE_TRIM_SETTINGS|DEEP_SLEEP_ENTRY|DEEP_SLEEP_EXIT|RESET_RECOVERY>`

Prerequisites: none

Description: This command is used to adapt the output voltage for internal regulators during handover
Please refer to specific Reference Manual of your Traveo II device to have full description of how this command works

#TPCMD OPEN_RMA

Syntax: `#TPCMD OPEN_RMA <UNIQUE ID0> <UNIQUE ID1> <UNIQUE ID2> <SRAM ADDRESS>`

Prerequisites: none

Description: This command enables the full access to the device in the RMA life-cycle stage upon successful execution
Please refer to specific Reference Manual of your Traveo II device to have full description of how this command works

#TPCMD TRANSITION_TO_RMA

Syntax: `#TPCMD TRANSITION_TO_RMA <UNIQUE ID0> <UNIQUE ID1> <UNIQUE ID2> <SRAM ADDRESS>`

Prerequisites: none

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Description: This command converts parts from secure or secure with debug state into the RMA life-cycle stage
Please refer to specific Reference Manual of your Traveo II device to have full description of how this command works

#TPCMD TRANSITION_TO_SECURE

Syntax: `#TPCMD TRANSITION_TO_SECURE <D|S> < SECURE_ACCESS_RESTRICT 32Bit> <DEAD_ACCESS_RESTRICT 32Bit>`

Prerequisites: none

Description: This command validates the FACTORY_HASH and programs the SECURE_HASH, secure access restrictions and dead access restrictions into eFUSE.
The first parameter of the command is <D|S>
D → SECURE_WITH_DEBUG life-cycle stage, with this parameter debuggers can read Flash memory and perform operations on Work Flash and read device information.
S → SECURE life-cycle stage

The second parameter is <SECURE_ACCESS_RESTRICT 32Bit>
For this parameter, please refer to specific Reference Manual of your Traveo II device

The third parameter is <DEAD_ACCESS_RESTRICT 32Bit>
For this parameter, please refer to specific Reference Manual of your Traveo II device

The new secure state is applied when a new Power on Reset is provided to the device. If you try to perform a new execution on the FlashRunner project with the command `#TPCMD GET_DEVICE_INFORMATIONS` it is possible to check the new life-cycle stage

NOTE: *This command can be performed only one time on same device because command writes eFUSE that are One Time Programmable values.*
For other information please refer to specific Reference Manual of the Traveo II device.
If you want to use the command `#TPCMD TRANSITION_TO_SECURE` remember to execute it as last operation before the `#TPCMD DISCONNECT` command.

#TPCMD READ_EFUSE_BYTE

Syntax: `#TPCMD READ_EFUSE_BYTE <Fuse byte [0-127]>`

Prerequisites: none

Description: This command allows to read a specific byte on the eFUSE memory area.

#TPCMD START_CPU

Syntax: `#TPCMD START_CPU <Time [s]>`

`<Time [s]>` Time in seconds (i.e., 2 s). This time is an optional parameter.

Prerequisites: none

Description: Move the Reset line up and down quickly to reset the device.
Then carry out the connection phase and reset the device again with a specific procedure for Traveo 2 devices.
`#TPCMD RUN <Time [s]>` after the procedure already described waits for the time entered.
This command typically can be used to execute the firmware programmed in the device.

Note: This command is available from **libtraveo2.so** version **5.09**

#TPCMD RUN

Syntax: `#TPCMD RUN <Time [s]>`

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	<Time [s]>	Time in seconds (i.e., 2 s). This time is an optional parameter.

Prerequisites: none

Description: Move the Reset line up and down quickly if no parameter <Time [s]> is inserted.
`#TPCMD RUN` <Time [s]> instead moves the Reset line down and high, waits for the entered time.
This command typically can be used to execute the firmware programmed in the device.

#TPCMD READ_MEM8

Syntax: `#TPCMD READ_MEM8` <Address> <Byte Count>

<Address>	Address in HEX format (i.e., 0x52002020)
<Byte Count>	Byte count in decimal format (i.e., 8 -> eight bytes)

Prerequisites: none

Description: Read memory byte per byte from target TRAVEO2 device

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM8 0x52002020 8
Read[0x52002020]: 0xF0
Read[0x52002021]: 0xAA
Read[0x52002022]: 0x16
Read[0x52002023]: 0x14
Read[0x52002024]: 0x00
Read[0x52002025]: 0x00
Read[0x52002026]: 0x00
Read[0x52002027]: 0x00
Time for Read Mem: 0.002 s
```


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#TPCMD READ_MEM16

Syntax: `#TPCMD READ_MEM16 <Address> <16-bit Word Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<16-bit Word Count>	16-bit Word count in decimal format (i.e., 4 -> four 16-bit words)

Prerequisites: none

Description: Read memory 16-bit word per 16-bit word from target TRAVEO2 device

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM16 0x52002020 4
Read[0x52002020]: 0xAAF0
Read[0x52002022]: 0x1416
Read[0x52002024]: 0x0000
Read[0x52002026]: 0x0000
Time for Read Mem: 0.002 s
```

#TPCMD READ_MEM32

Syntax: `#TPCMD READ_MEM32 <Address> <32-bit Word Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<32-bit Word Count>	32-bit Word count in decimal format (i.e., 2 -> two 32-bit words)

Prerequisites: none

Description: Read memory 32-bit word per 32-bit word from target TRAVEO2 device

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM32 0x52002020 2
Read[0x52002020]: 0x1416AAF0
Read[0x52002024]: 0x00000000
Time for Read Mem: 0.002 s
```

#TPCMD DISCONNECT

`#TPCMD DISCONNECT`

Disconnect function. Power off and exit.

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INFINEON TRAVEO2 Driver Examples

Here you can see a complete example of INFINEON TRAVEO2 projects.

1 – INFINEON TRAVEO2 4.06 MB example Commands

```
#TCSETPAR ACQUIRING_SEQUENCE ACQUIRE_CHIP
#TCSETPAR ENTRY_CLOCK 1000000
#TCSETPAR PROTCLK 37500000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV PUSHPULL
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 5000
#TCSETPAR CMODE SWD
#TPSETSRC 4_06MB.frb
#TPSTART
#TPCMD CONNECT
#IFERR TPCMD BLANKCHECK F
#THEN TPCMD MASSERASE F
#THEN TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TPCMD DISCONNECT
#TPEND
```

1 – INFINEON TRAVEO2 4.06 MB example Real Time Log

```
---#TPSTART
Load SWD FPGA version 0x00001215.
Detected Traveo II device: TRAVEO™ II body high MCU.
Selected Traveo II Acquire Sequence.
>|
---#TPCMD CONNECT
Protocol selected SWD.
Toggling XRES pin to execute Acquire Chip procedure.
ID-Code read correctly at 1.00 MHz after 12 retries.
JTAG-SWD Debug Port enabled.
Move Traveo II internal state to Test Mode.
Traveo II enter into Test Mode.
Scanning AP map to find all APs:
 * AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[1] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[2] IDR: 0x24770011, Type: AMBA AHB3 bus.
Scanning AP to find all cores:
 * AP[1] Found Cortex M0+ revision r0p1.
         CPUID: 0x410CC601.
         Implementer Code: 0x41 - [ARM].
         ROM table base address 0xF0000000.
 * AP[2] Found Cortex M4 revision r0p1.
         CPUID: 0x410FC241.
         Implementer Code: 0x41 - [ARM].
         ROM table base address 0xE00FF000.
Try to halt the Cortex M0+ core:
 * AP[1] Cortex M0+ Core halted [0.001 s].
Try to halt the Cortex M4 core:
 * AP[2] Cortex M4 Core halted [0.001 s].
Try to execute the Acquire Chip method procedure:
 * AP[1] Cortex M0+ core Vector Table base 0x00000000.
 * Vector Table value means that the Flash is empty or TOC is corrupted.
 * Acquire Chip method procedure completed.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 4 [Range 4-7].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Read device informations:
 * FamilyId: 0x0108.
 * Revision: 0x11.
```


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```
 * SiliconID: 0xEA06.
 * Protect state: 0x2: Virgin - [NORMAL] - Secure - Dead.
 * Life cycle stage: 0x7 - Normal Provisioned.
 * Flash boot version: 0xA301.
 * SROM firmware version: 0x0601.
Read device unique ID:
 * Unique ID0: 0x0089A27F, Unique ID1: 0xFF272F10, Unique ID2: 0x79030800.
Normal device access restrictions:
 * Enabled Cortex M0-AP access.
 * Enabled Cortex CM7 n.0/CM7 n.1 AP access.
 * Enabled system AP access.
 * MPU is locked, all SRAM is accessible.
 * Enabled Direct Execute system call functionality.
 * Entire Flash main region is accessible.
 * Entire SRAM main region is accessible.
 * Entire Work Flash main region is accessible.
 * Entire Supervisory Flash main region is accessible.
> Check Traveo II Silicon ID passed from SMH database [0xEA06].
* Check Traveo II Silicon ID from source file not available.
Time for Connect: 0.308 s.
>|
---#IFERR TPCMD BLANKCHECK F
Time for Blankcheck F: 0.110 s.
>|
---#TPCMD PROGRAM F
Default Single Bank mode for Flash memory.
Start Program operation.
Time for Program F: 3.242 s.
>|
---#TPCMD VERIFY F R
Default Single Bank mode for Flash memory.
Start Verify Readout operation.
Time for Verify Readout F: 1.668 s.
>|
---#TPCMD VERIFY F S
Default Single Bank mode for Flash memory.
Start Verify Checksum 32bit operation.
Time for Verify Checksum 32bit F: 0.079 s.
>|
---#TPCMD DISCONNECT
>|
```

1 – INFINEON TRAVEO2 4.06 MB example Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.308 s
Conditional Blankcheck Flash	0.110 s
Program Flash	3.242 s
Verify Readout Flash	1.668 s
Verify Checksum Flash	0.079 s
Cycle Time	**00:05.662 s**

2 – INFINEON TRAVEO2 4.06 MB example Commands

```
#TCSETPAR ACQUIRING_SEQUENCE ACQUIRE_CHIP
#TCSETPAR ENTRY_CLOCK 1000000
#TCSETPAR PROTCLK 37500000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV PUSHPULL
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 5000
#TCSETPAR CMODE SWD
#TPSETSRC 4_06MB.frb
```


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```
#TPSTART
#TPCMD CONNECT
#IFERR TPCMD BLANKCHECK F
#THEN TPCMD MASSERASE F
#THEN TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TPCMD DISCONNECT
#TPEND
```

2 – INFINEON TRAVEO2 4.06 MB example Real Time Log

```
---#TPSTART
Load SWD FPGA version 0x00001215.
Detected Traveo II device: TRAVEO™ II body high MCU.
Selected Traveo II Acquire Sequence.
>|
---#TPCMD CONNECT
Error turning on VPROG0. Setting voltage gradually to limit the peak of current.
Protocol selected SWD.
Toggling XRES pin to execute Acquire Chip procedure.
ID-Code read correctly at 1.00 MHz after 12 retries.
JTAG-SWD Debug Port enabled.
Move Traveo II internal state to Test Mode.
Traveo II enter into Test Mode.
Scanning AP map to find all APs:
 * AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[1] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[2] IDR: 0x24770011, Type: AMBA AHB3 bus.
Scanning AP to find all cores:
 * AP[1] Found Cortex M0+ revision r0p1.
         CPUID: 0x410CC601.
         Implementer Code: 0x41 - [ARM].
         ROM table base address 0xF0000000.
 * AP[2] Found Cortex M4 revision r0p1.
         CPUID: 0x410FC241.
         Implementer Code: 0x41 - [ARM].
         ROM table base address 0xE00FF000.
Try to halt the Cortex M0+ core:
 * AP[1] Cortex M0+ Core halted [0.001 s].
Try to halt the Cortex M4 core:
 * AP[2] Cortex M4 Core halted [0.002 s].
Try to execute the Acquire Chip method procedure:
 * AP[1] Cortex M0+ core Vector Table base 0x00000000.
 * Vector Table value means that the Flash is empty or TOC is corrupted.
 * Acquire Chip method procedure completed.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 4 [Range 4-7].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Read device informations:
 * FamilyId: 0x0108.
 * Revision: 0x11.
 * SiliconID: 0xEA06.
 * Protect state: 0x2: Virgin - [NORMAL] - Secure - Dead.
 * Life cycle stage: 0x7 - Normal Provisioned.
 * Flash boot version: 0xA301.
 * SROM firmware version: 0x0601.
Read device unique ID:
 * Unique ID0: 0x0089A27F, Unique ID1: 0xFF272F10, Unique ID2: 0x79030800.
Normal device access restrictions:
 * Enabled Cortex M0-AP access.
 * Enabled Cortex CM7 n.0/CM7 n.1 AP access.
 * Enabled system AP access.
 * MPU is locked, all SRAM is accessible.
 * Enabled Direct Execute system call functionality.
 * Entire Flash main region is accessible.
 * Entire SRAM main region is accessible.
 * Entire Work Flash main region is accessible.
 * Entire Supervisory Flash main region is accessible.
> Check Traveo II Silicon ID passed from SMH database [0xEA06].
* Check Traveo II Silicon ID from source file not available.
Time for Connect: 0.508 s.
>|
```


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```
---#IFERR TPCMD BLANKCHECK F
Address of first not blank location: 0x10000000.
Value read at address 0x10000000 is 0x7B146816.
0800A323!|
---#THEN TPCMD MASSERASE F
Time for Masserase F: 7.137 s.
>|
---#THEN TPCMD BLANKCHECK F
Time for Blankcheck F: 0.110 s.
>|
---#TPCMD PROGRAM F
Default Single Bank mode for Flash memory.
Start Program operation.
Time for Program F: 3.242 s.
>|
---#TPCMD VERIFY F R
Default Single Bank mode for Flash memory.
Start Verify Readout operation.
Time for Verify Readout F: 1.668 s.
>|
---#TPCMD VERIFY F S
Default Single Bank mode for Flash memory.
Start Verify Checksum 32bit operation.
Time for Verify Checksum 32bit F: 0.091 s.
>|
---#TPCMD DISCONNECT
>|
```

2 – INFINEON TRAVEO2 4.06 MB example Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.308 s
Conditional Blankcheck Flash	0.010 s
Conditional Masserase Flash	7.137 s
Conditional Blankcheck Flash	0.110 s
Program Flash	3.242 s
Verify Readout Flash	1.668 s
Verify Checksum Flash	0.079 s
Cycle Time	**00:12.817 s**

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3 – INFINEON TRAVEO2 8.19 MB example Commands

```
#TCSETPAR ACQUIRING_SEQUENCE ACQUIRE_CHIP
#TCSETPAR ENTRY_CLOCK 1000000
#TCSETPAR PROTCLK 37500000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV OPENDRAIN
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 5000
#TCSETPAR CMODE SWD
#TPSETSRC 8_19MB.frb
#TPSTART
#TPCMD CONNECT
#IFERR TPCMD BLANKCHECK F
#THEN TPCMD MASSERASE F
#THEN TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TPCMD DISCONNECT
#TPEND
```

3 – INFINEON TRAVEO2 8.19 MB example Real Time Log

```
---#TPSTART
Load SWD FPGA version 0x00001215.
Detected Traveo II device: TRAVEO™ II body high MCU.
Selected Traveo II Acquire Sequence.
>|
---#TPCMD CONNECT
Protocol selected SWD.
Toggling XRES pin to execute Acquire Chip procedure.
ID-Code read correctly at 1.00 MHz after 17 retries.
JTAG-SWD Debug Port enabled.
Move Traveo II internal state to Test Mode.
Traveo II enter into Test Mode.
Scanning AP map to find all APs:
 * AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[1] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[2] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[3] IDR: 0x84770001, Type: AMBA AHB3 bus.
Scanning AP to find all cores:
 * AP[1] Found Cortex M0+ revision r0p1.
         CPUID: 0x410CC601.
         Implementer Code: 0x41 - [ARM].
         ROM table base address 0xF0000000.
 * AP[2] Found Cortex M7 revision r1p2.
         CPUID: 0x411FC272.
         Implementer Code: 0x41 - [ARM].
         ROM table base address 0xE00FE000.
 * AP[3] Found Cortex M7 revision r1p2.
         CPUID: 0x411FC272.
         Implementer Code: 0x41 - [ARM].
         ROM table base address 0xE00FE000.
Try to halt the Cortex M0+ core:
 * AP[1] Cortex M0+ Core halted [0.002 s].
Try to halt the Cortex M7 core:
 * AP[2] Cortex M7 Core halted [0.001 s].
Try to halt the Cortex M7 core:
 * AP[3] Cortex M7 Core halted [0.001 s].
Try to execute the Acquire Chip method procedure:
 * AP[1] Cortex M0+ core Vector Table base 0x00000000.
 * Vector Table value means that the Flash is empty or TOC is corrupted.
 * Acquire Chip method procedure completed.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 3 [Range 5-7].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Read device informations:
 * FamilyId: 0x0103.
 * Revision: 0x23.
```


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```
 * SiliconID: 0xE5EB.
 * Protect state: 0x2: Virgin - [NORMAL] - Secure - Dead.
 * Life cycle stage: 0x7 - Normal Provisioned.
 * Flash boot version: 0xA301.
 * SROM firmware version: 0x0701.
Read device unique ID:
 * Unique ID0: 0x0089B5F1, Unique ID1: 0xFF101A02, Unique ID2: 0x780B0D00.
Normal device access restrictions:
 * Enabled Cortex M0-AP access.
 * Enabled Cortex CM7 n.0/CM7 n.1 AP access.
 * Enabled system AP access.
 * MPU is locked, all SRAM is accessible.
 * Enabled Direct Execute system call functionality.
 * Entire Flash main region is accessible.
 * Entire SRAM main region is accessible.
 * Entire Work Flash main region is accessible.
 * Entire Supervisory Flash main region is accessible.
> Check Traveo II Silicon ID passed from SMH database [0xE5EB].
FRB CRC32 check passed.
FRB Headers collected.
* Check Traveo II Silicon ID from source file not available.
Time for Connect: 0.324 s.
>|
---#IFERR TPCMD BLANKCHECK F
Time for Blankcheck F: 0.442 s.
>|
---#TPCMD PROGRAM F
Default Single Bank mode for Flash memory.
Start Program operation.
Time for Program F: 14.272 s.
>|
---#TPCMD VERIFY F R
Default Single Bank mode for Flash memory.
Start Verify Readout operation.
Time for Verify Readout F: 3.359 s.
>|
---#TPCMD VERIFY F S
Default Single Bank mode for Flash memory.
Start Verify Checksum 32bit operation.
Time for Verify Checksum 32bit F: 0.314 s.
>|
---#TPCMD DISCONNECT
>|
```

3 – INFINEON TRAVEO2 8.19 MB example Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.324 s
Conditional Blankcheck Flash	0.442 s
Program Flash	14.272 s
Verify Readout Flash	3.359 s
Verify Checksum Flash	0.314 s
Cycle Time	**00:18.771 s**

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4 – INFINEON TRAVEO2 8.19 MB example Commands

```
#TCSETPAR ACQUIRING_SEQUENCE ACQUIRE_CHIP
#TCSETPAR ENTRY_CLOCK 1000000
#TCSETPAR PROTCLK 37500000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV OPENDRAIN
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 5000
#TCSETPAR CMODE SWD
#TPSETSRC 8_19MB.frb
#TPSTART
#TPCMD CONNECT
#IFERR TPCMD BLANKCHECK F
#THEN TPCMD MASSERASE F
#THEN TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TPCMD DISCONNECT
#TPEND
```

4 – INFINEON TRAVEO2 8.19 MB example Real Time Log

```
---#TPSTART
Load SWD FPGA version 0x00001215.
Detected Traveo II device: TRAVEO™ II body high MCU.
Selected Traveo II Acquire Sequence.
>|
---#TPCMD CONNECT
Protocol selected SWD.
Toggling XRES pin to execute Acquire Chip procedure.
ID-Code read correctly at 1.00 MHz after 19 retries.
JTAG-SWD Debug Port enabled.
Move Traveo II internal state to Test Mode.
Traveo II enter into Test Mode.
Scanning AP map to find all APs:
 * AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[1] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[2] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[3] IDR: 0x84770001, Type: AMBA AHB3 bus.
Scanning AP to find all cores:
 * AP[1] Found Cortex M0+ revision r0p1.
         CPUID: 0x410CC601.
         Implementer Code: 0x41 - [ARM].
         ROM table base address 0xF0000000.
 * AP[2] Found Cortex M7 revision r1p2.
         CPUID: 0x411FC272.
         Implementer Code: 0x41 - [ARM].
         ROM table base address 0xE00FE000.
 * AP[3] Found Cortex M7 revision r1p2.
         CPUID: 0x411FC272.
         Implementer Code: 0x41 - [ARM].
         ROM table base address 0xE00FE000.
Try to halt the Cortex M0+ core:
 * AP[1] Cortex M0+ Core halted [0.001 s].
Try to halt the Cortex M7 core:
 * AP[2] Cortex M7 Core halted [0.002 s].
Try to halt the Cortex M7 core:
 * AP[3] Cortex M7 Core halted [0.002 s].
Try to execute the Acquire Chip method procedure:
 * AP[1] Cortex M0+ core Vector Table base 0x00000000.
 * Vector Table value means that the Flash is empty or TOC is corrupted.
 * Acquire Chip method procedure completed.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 3 [Range 5-7].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Read device informations:
 * FamilyId: 0x0103.
 * Revision: 0x23.
```


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```
 * SiliconID: 0xE5EB.
 * Protect state: 0x2: Virgin - [NORMAL] - Secure - Dead.
 * Life cycle stage: 0x7 - Normal Provisioned.
 * Flash boot version: 0xA301.
 * SROM firmware version: 0x0701.
Read device unique ID:
 * Unique ID0: 0x0089B5F1, Unique ID1: 0xFF101A02, Unique ID2: 0x780B0D00.
Normal device access restrictions:
 * Enabled Cortex M0-AP access.
 * Enabled Cortex CM7 n.0/CM7 n.1 AP access.
 * Enabled system AP access.
 * MPU is locked, all SRAM is accessible.
 * Enabled Direct Execute system call functionality.
 * Entire Flash main region is accessible.
 * Entire SRAM main region is accessible.
 * Entire Work Flash main region is accessible.
 * Entire Supervisory Flash main region is accessible.
> Check Traveo II Silicon ID passed from SMH database [0xE5EB].
* Check Traveo II Silicon ID from source file not available.
Time for Connect: 0.165 s.
>|
---#IFERR TPCMD BLANKCHECK F
Address of first not blank location: 0x10000000.
Value read at address 0x10000000 is 0x7B146816.
0800A323!|
---#THEN TPCMD MASSERASE F
Time for Masserase F: 14.254 s.
>|
---#THEN TPCMD BLANKCHECK F
Time for Blankcheck F: 0.441 s.
>|
---#TPCMD PROGRAM F
Default Single Bank mode for Flash memory.
Start Program operation.
Time for Program F: 14.272 s.
>|
---#TPCMD VERIFY F R
Default Single Bank mode for Flash memory.
Start Verify Readout operation.
Time for Verify Readout F: 3.359 s.
>|
---#TPCMD VERIFY F S
Default Single Bank mode for Flash memory.
Start Verify Checksum 32bit operation.
Time for Verify Checksum 32bit F: 0.315 s.
>|
---#TPCMD DISCONNECT
>|
```

4 – INFINEON TRAVEO2 8.19 MB example Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.308 s
Conditional Blankcheck Flash	0.010 s
Conditional Masserase Flash	14.254 s
Conditional Blankcheck Flash	0.441 s
Program Flash	14.272 s
Verify Readout Flash	3.359 s
Verify Checksum Flash	0.315 s
Cycle Time	**00:32.867 s**

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5 – INFINEON TRAVEO2 16.38 MB + 512KB + 64 KB example Commands

```
#TCSETPAR ACQUIRING_SEQUENCE ACQUIRE_CHIP
#TCSETPAR ENTRY_CLOCK 1000000
#TCSETPAR PROTCLK 37500000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV OPENDRAIN
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 5000
#TCSETPAR CMODE SWD
#TPSETSRC ALL.frb
#TPSTART
#TPCMD CONNECT
#TPCMD CONNECT
#TPCMD MASSERASE F
#TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TPCMD MASSERASE E
#TPCMD BLANKCHECK E
#TPCMD PROGRAM E
#TPCMD VERIFY E R
#TPCMD VERIFY E S
#TPCMD MASSERASE T
#TPCMD BLANKCHECK T
#TPCMD PROGRAM T
#TPCMD VERIFY T R
#TPCMD VERIFY T S
#TPCMD DISCONNECT
#TPEND
```

5 – INFINEON TRAVEO2 16.38 MB + 512KB + 64 KB example Real Time Log

```
---#TPSTART
Load SWD FPGA version 0x00001215.
Detected Traveo II device: TRAVEO™ II Body Controller High MCU.
Selected Traveo II Acquire Sequence.
>|
---#TPCMD CONNECT
Protocol selected SWD.
Toggling XRES pin to execute Acquire Chip procedure.
ID-Code read correctly at 4.00 MHz after 49 retries.
JTAG-SWD Debug Port enabled.
Move Traveo II internal state to Test Mode.
Traveo II enter into Test Mode.
Scanning AP map to find all APs:
 * AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[1] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[2] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[3] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[4] IDR: 0x84770001, Type: AMBA AHB3 bus.
 * AP[5] IDR: 0x84770001, Type: AMBA AHB3 bus.
Scanning AP to find all cores:
 * AP[1] ARM - CPUID: 0x410CC601 - Found Cortex M0+ revision r0p1.
 * AP[2] ARM - CPUID: 0x411FC272 - Found Cortex M7 revision r1p2.
 * AP[3] ARM - CPUID: 0x411FC272 - Found Cortex M7 revision r1p2.
 * AP[4] ARM - CPUID: 0x411FC272 - Found Cortex M7 revision r1p2.
 * AP[5] ARM - CPUID: 0x411FC272 - Found Cortex M7 revision r1p2.
Try to halt the Cortex M0+ core:
 * AP[1] Cortex M0+ core halted after 0.002 s.
 * AP[1] Cortex M0+ core Program Counter is 0x000003D2.
Try to halt the Cortex M7 core:
 * AP[2] Cortex M7 core halted after 0.001 s.
 * AP[1] Cortex M0+ core Program Counter is 0x00000128.
Try to halt the Cortex M7 core:
 * AP[3] Cortex M7 core halted after 0.001 s.
 * AP[1] Cortex M0+ core Program Counter is 0x00000218.
Try to halt the Cortex M7 core:
 * AP[4] Cortex M7 core halted after 0.001 s.
 * AP[1] Cortex M0+ core Program Counter is 0x0000012E.
Try to halt the Cortex M7 core:
```


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```
 * AP[5] Cortex M7 core halted after 0.001 s.
 * AP[1] Cortex M0+ core Program Counter is 0x00000266.
Try to execute the Acquire Chip method procedure:
 * AP[1] Cortex M0+ core Program Counter is 0x000003D2.
 * AP[1] Cortex M0+ core Vector Table base 0xFFFF0000.
 * Vector Table value means that the Flash is empty or TOC is corrupted.
> Acquire Chip method procedure completed.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 4 [Range 4-7].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Read device informations:
 * FamilyId: 0x0114.
 * Revision: 0x11.
 * SiliconID: 0xED04.
 * Protect state: 0x2: Virgin - [NORMAL] - Secure - Dead.
 * Life cycle stage: 0x7 - Normal Provisioned.
 * Flash boot version: 0xA301.
 * SROM firmware version: 0x0801.
Read device unique ID:
 * Unique ID0: 0x008D24EC, Unique ID1: 0xFF0A0504, Unique ID2: 0x7C090600.
Normal device access restrictions:
 * Enabled Cortex M0-AP access.
 * Enabled Cortex CM7 n.0/CM7 n.1 AP access.
 * Enabled system AP access.
 * MPU is locked, all SRAM is accessible.
 * Enabled Direct Execute system call functionality.
 * Entire Flash main region is accessible.
 * Entire SRAM main region is accessible.
 * Entire Work Flash main region is accessible.
 * Entire Supervisory Flash main region is accessible.
> Check Traveo II Silicon ID passed from SMH database [0xED04].
* Check Traveo II Silicon ID from source file not available.
Time for Connect: 0.510 s.
>|
---#TPCMD MASSERASE F
Start Masserase operation for Flash memory region 0.
> Completed Masserase operation.
Start Masserase operation for Flash memory region 1.
> Completed Masserase operation.
Time for Masserase F: 23.375 s.
>|
---#TPCMD BLANKCHECK F
Start Blankcheck operation for Flash memory region 0.
> Completed Blankcheck operation.
Start Blankcheck operation for Flash memory region 1.
> Completed Blankcheck operation.
Time for Blankcheck F: 0.441 s.
>|
---#TPCMD PROGRAM F
Start Program operation for Flash memory region 0.
 * Default Single Bank mode for Flash memory.
> Completed Program operation.
Start Program operation for Flash memory region 1.
 * Default Single Bank mode for Flash memory.
> Completed Program operation.
Time for Program F: 6.723 s.
>|
---#TPCMD VERIFY F R
Start Verify Readout operation for Flash memory region 0.
 * Default Single Bank mode for Flash memory.
> Completed Verify Readout operation.
Start Verify Readout operation for Flash memory region 1.
 * Default Single Bank mode for Flash memory.
> Completed Verify Readout operation.
Time for Verify Readout F: 6.718 s.
>|
---#TPCMD VERIFY F S
Start Verify Checksum 32bit operation for Flash memory region 0.
 * Default Single Bank mode for Flash memory.
> Completed Verify Checksum 32bit operation.
Start Verify Checksum 32bit operation for Flash memory region 1.
 * Default Single Bank mode for Flash memory.
> Completed Verify Checksum 32bit operation.
Time for Verify Checksum 32bit F: 0.317 s.
>|
---#TPCMD MASSERASE E
Start Erase operation for Work Flash memory region 0.
```


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```
 * Large sectors size 2KB, small sectors size 128B.
 * Large sectors number 96, small sectors number 512.
> Completed Masserase operation.
Start Erase operation for Work Flash memory region 1.
 * Large sectors size 2KB, small sectors size 128B.
 * Large sectors number 96, small sectors number 512.
> Completed Masserase operation.
Time for Masserase E: 9.706 s.
>|
---#TPCMD BLANKCHECK E
Start Blankcheck operation for Work Flash memory region 0.
> Completed Blankcheck operation.
Start Blankcheck operation for Work Flash memory region 1.
> Completed Blankcheck operation.
Time for Blankcheck E: 0.312 s.
>|
---#TPCMD PROGRAM E
Start Program operation for Work Flash memory region 0.
 * Default Single Bank mode for Work Flash memory.
> Completed Program operation.
Start Program operation for Work Flash memory region 1.
 * Default Single Bank mode for Work Flash memory.
> Completed Program operation.
Time for Program E: 13.052 s.
>|
---#TPCMD VERIFY E R
Start Verify Readout operation for Work Flash memory region 0.
 * Default Single Bank mode for Work Flash memory.
> Completed Verify Readout operation.
Start Verify Readout operation for Work Flash memory region 1.
 * Default Single Bank mode for Work Flash memory.
> Completed Verify Readout operation.
Time for Verify Readout E: 0.273 s.
>|
---#TPCMD VERIFY E S
Start Verify Checksum 32bit operation for Work Flash memory region 0.
 * Default Single Bank mode for Work Flash memory.
> Completed Verify Checksum 32bit operation.
Start Verify Checksum 32bit operation for Work Flash memory region 1.
 * Default Single Bank mode for Work Flash memory.
> Completed Verify Checksum 32bit operation.
Time for Verify Checksum 32bit E: 0.111 s.
>|
---#TPCMD MASSERASE T
Start Erase operation for Extended Code Flash memory region 0.
> Completed Masserase operation.
Start Erase operation for Extended Code Flash memory region 1.
> Completed Masserase operation.
Time for Masserase T: 0.115 s.
>|
---#TPCMD BLANKCHECK T
Start Blankcheck operation for Extended Code Flash memory region 0.
> Completed Blankcheck operation.
Start Blankcheck operation for Extended Code Flash memory region 1.
> Completed Blankcheck operation.
Time for Blankcheck T: 0.002 s.
>|
---#TPCMD PROGRAM T
Start Program operation for Extended Code Flash memory region 0.
> Completed Program operation.
Start Program operation for Extended Code Flash memory region 1.
> Completed Program operation.
Time for Program T: 0.043 s.
>|
---#TPCMD VERIFY T R
Start Verify Readout operation for Extended Code Flash memory region 0.
> Completed Verify Readout operation.
Start Verify Readout operation for Extended Code Flash memory region 1.
> Completed Verify Readout operation.
Time for Verify Readout T: 0.028 s.
>|
---#TPCMD VERIFY T S
Start Verify Checksum 32bit operation for Extended Code Flash memory region 0.
> Completed Verify Checksum 32bit operation.
Start Verify Checksum 32bit operation for Extended Code Flash memory region 1.
> Completed Verify Checksum 32bit operation.
Time for Verify Checksum 32bit T: 0.003 s.
>|
---#TPCMD DISCONNECT
>|
```


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5 – INFINEON TRAVEO2 16.38 MB + 512KB + 64 KB example Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.510 s
Masserase Flash	23.375 s
Blankcheck Flash	0.441 s
Program Flash	6.723 s
Verify Readout Flash	6.718 s
Verify Checksum Flash	0.317 s
Masserase WorkFlash	9.706 s
Blankcheck WorkFlash	0.312 s
Program WorkFlash	13.052 s
Verify Readout WorkFlash	0.273 s
Verify Checksum WorkFlash	0.111 s
Masserase Extended Code Flash	0.115 s
Blankcheck Extended Code Flash	0.002 s
Program Extended Code Flash	0.043 s
Verify Readout Extended Code Flash	0.028 s
Verify Checksum Extended Code Flash	0.003 s
Cycle Time	**01:03.103 s**

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INFINEON TRAVEO2 Driver Changelog

Info about driver versions prior to 5.00
All driver versions prior to 5.00 are to be considered obsolete, please update your driver to the latest version.

Info about driver version 5.00 - 10/03/2023
Upgraded Traveo2 driver.

Info about driver version 5.01 - 24/03/2023
Fixed wrong print into connect procedure when Acquire Chip is selected.
Upgrade management for Hyperflash memory programming through Traveo II device.

Info about driver version 5.02 - 15/06/2023
Upgraded Supervisory - Work Flash Program and Verify procedure when there are discontinued data blocks into FRB file.

Info about driver version 5.03 - 19/06/2023
Internal upgrade for dump command.

Info about driver version 5.04 - 06/09/2023
Internal driver upgrade.

Info about driver version 5.05 - 08/09/2023
Managed retro compatibility for Metadata Memory [M] with previous Reserved Memory [R].

Info about driver version 5.06 - 08/09/2023
Managed retro compatibility for very old projects where Traveo II Silicon ID is missing.

Info about driver version 5.07 - 12/01/2024
Updated Work Flash Masserase operation for CYT3DL Traveo II devices.

Info about driver version 5.08 - 02/04/2024
Updated Reset hardware management during Connect operation.

Info about driver version 5.09 - 08/07/2024
Added new #TPCMD START_CPU command.

Info about driver version 5.10 - 04/11/2024
Added new Traveo II devices.
Updated again Reset hardware management during Connect operation.

Info about driver version 5.11 - 03/12/2024
Automatically skipped reserved areas for Supervisory memory for Program and Verify operations.
The addresses available for the supervision memory are:

```
0x17000800 -> Row 4  - User Area
0x17000A00 -> Row 5  - User Area
0x17000C00 -> Row 6  - User Area
0x17000E00 -> Row 7  - User Area
0x17001A00 -> Row 13 - N/D AR
0x17006400 -> Row 50 - Public Key
0x17006600 -> Row 51 - Public Key
0x17006800 -> Row 52 - Public Key
0x17006A00 -> Row 53 - Public Key
0x17006C00 -> Row 54 - Public Key
0x17006E00 -> Row 55 - Public Key
0x17007600 -> Row 59 - App Prot
0x17007C00 -> Row 62 - TOC 2
```

Info about driver version 5.12 - 07/03/2025
Added new CYT6BJBxx Traveo II devices.
Updated hardware breakpoint procedure for Connect operation.
Updated print into Connect operation and standard commands.

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